@EchelleInconnue
@VentresMous

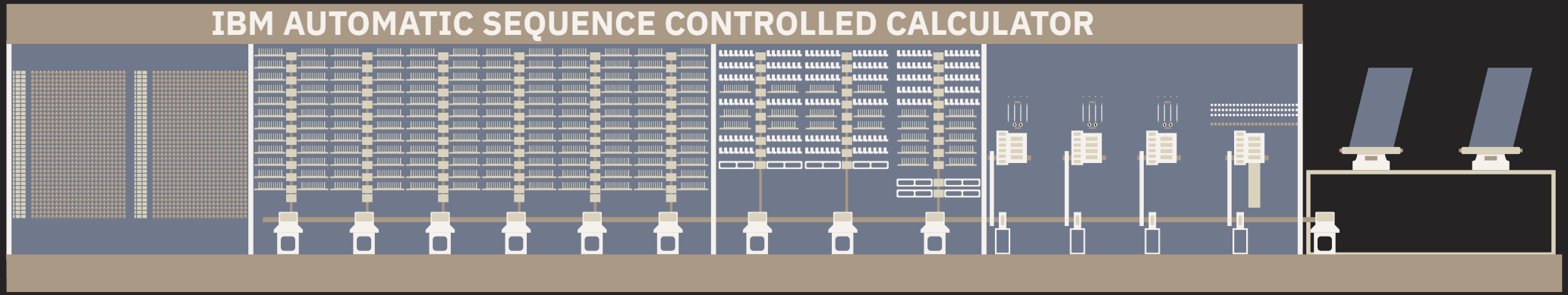
FPGA

Créer du matériel en programmant

SOMMAIRE

IL ÉTAIT UNE FOIS : LES CPU

15,5 mètres



constantes

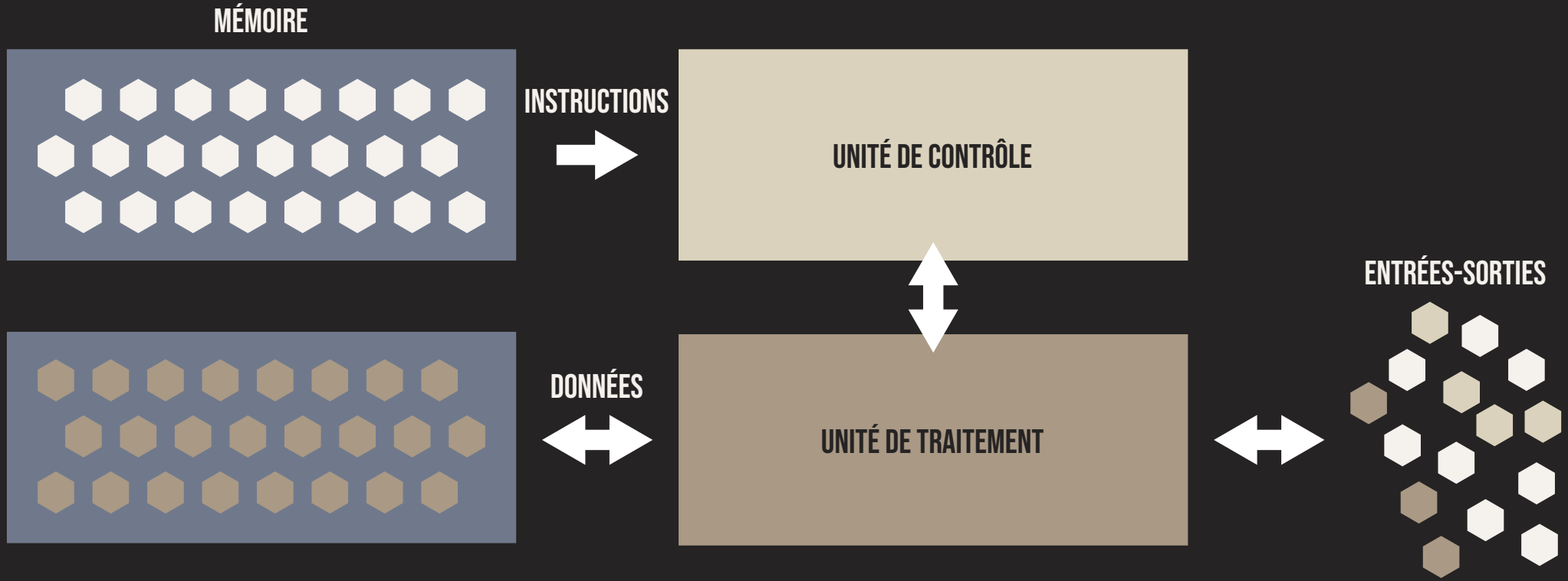
mémoire de données

unité de traitement

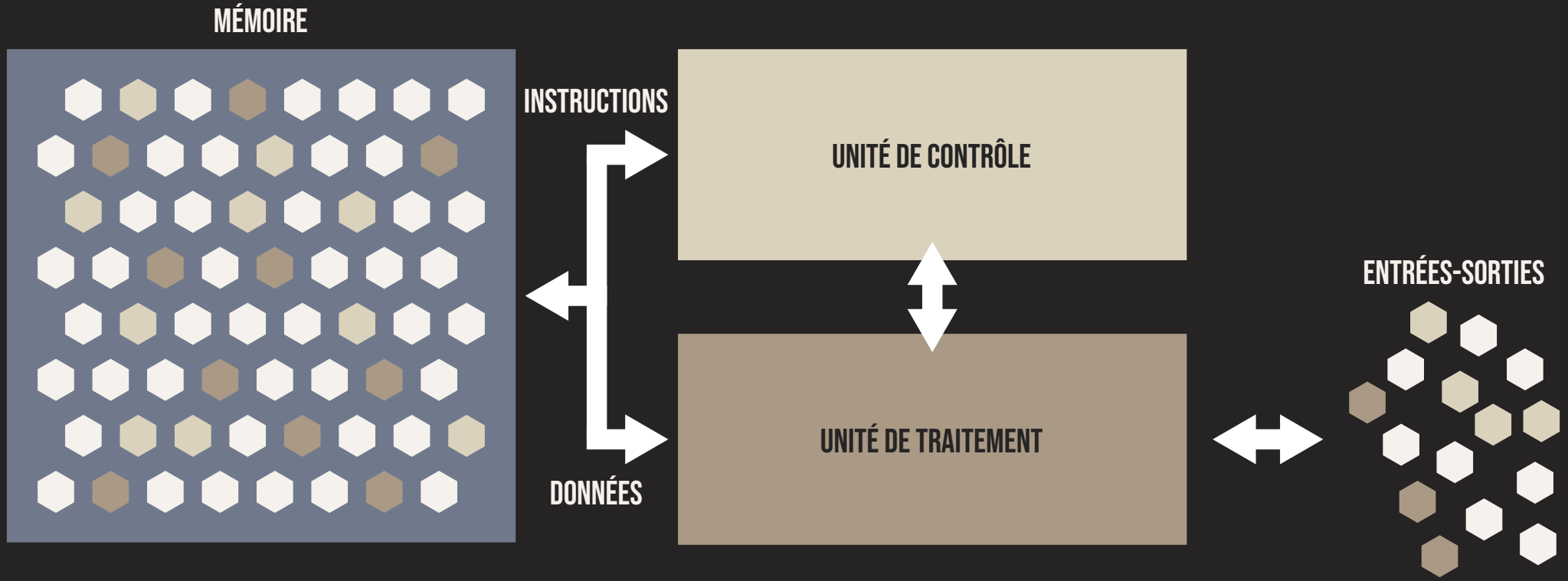
unité de contrôle
mémoire d'instructions

entrées/sorties

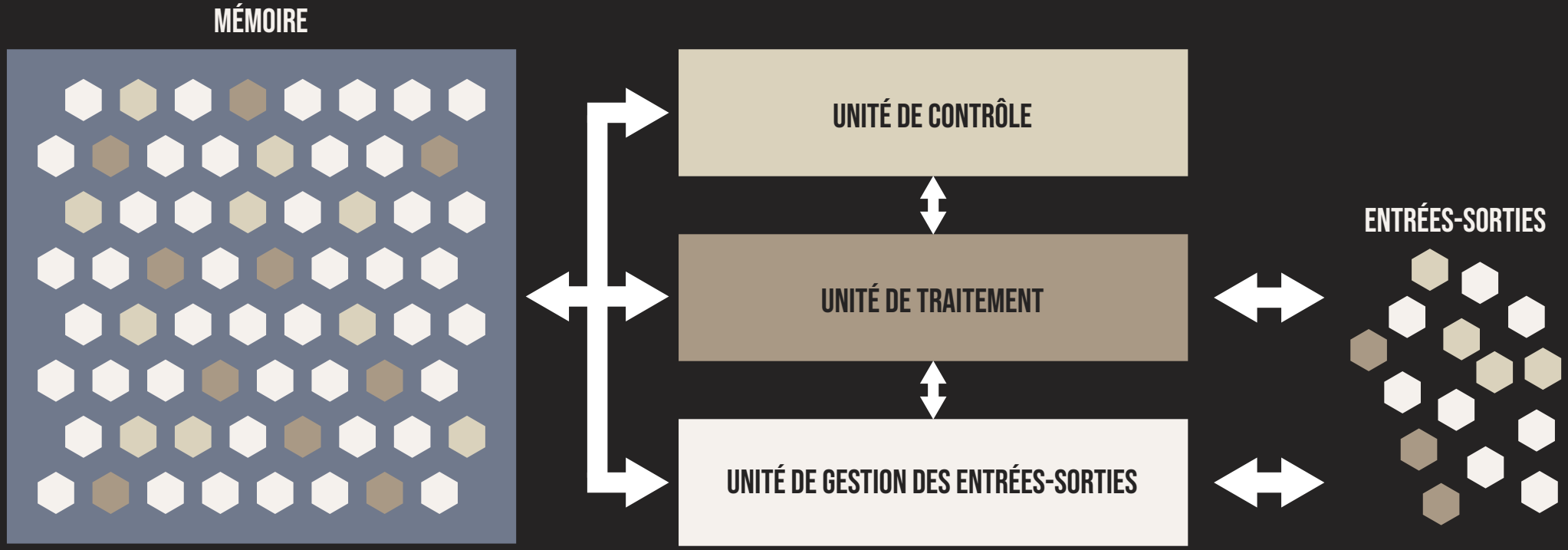
HARVARD MARK I, 1944



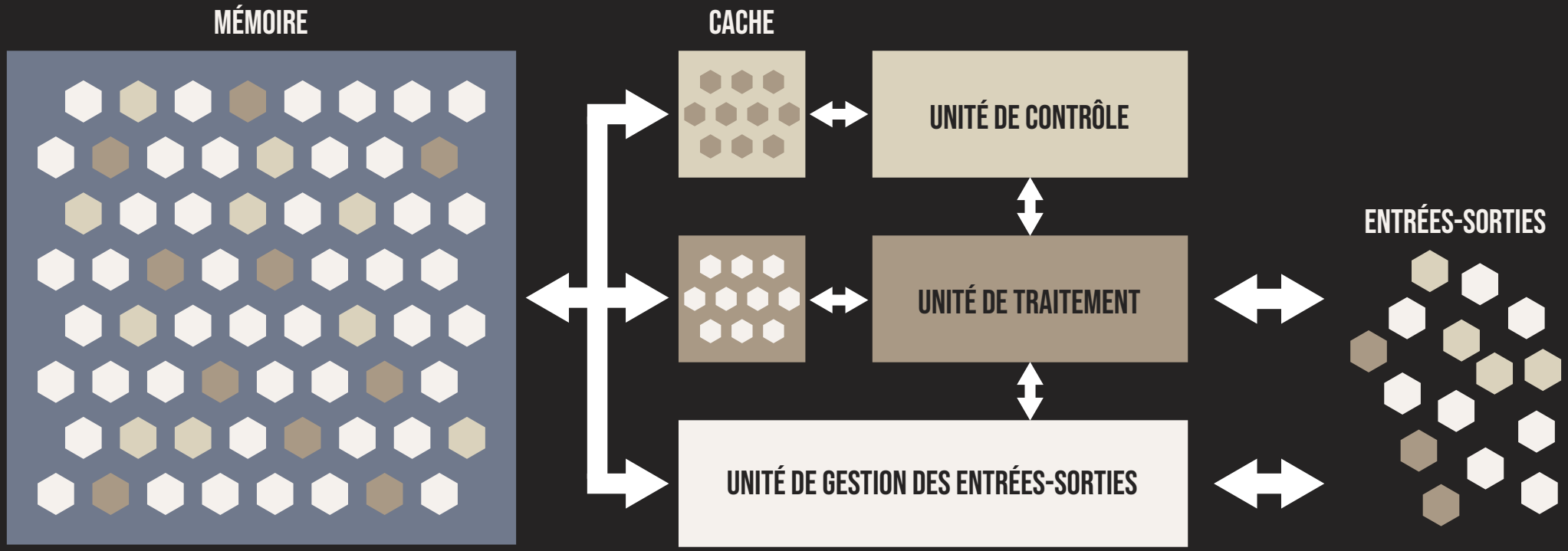
ARCHITECTURE HARVARD



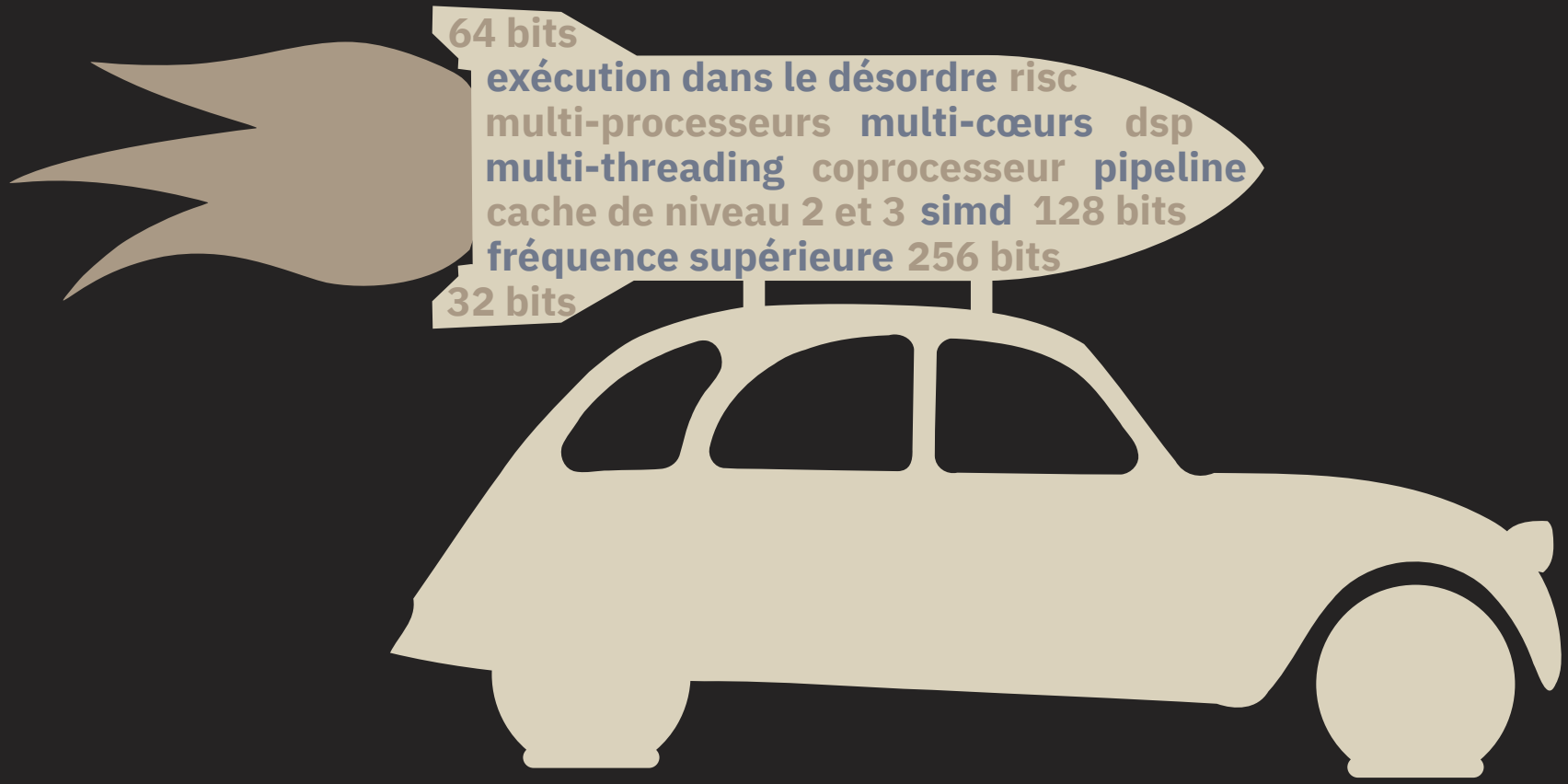
ARCHITECTURE DE VON NEUMANN



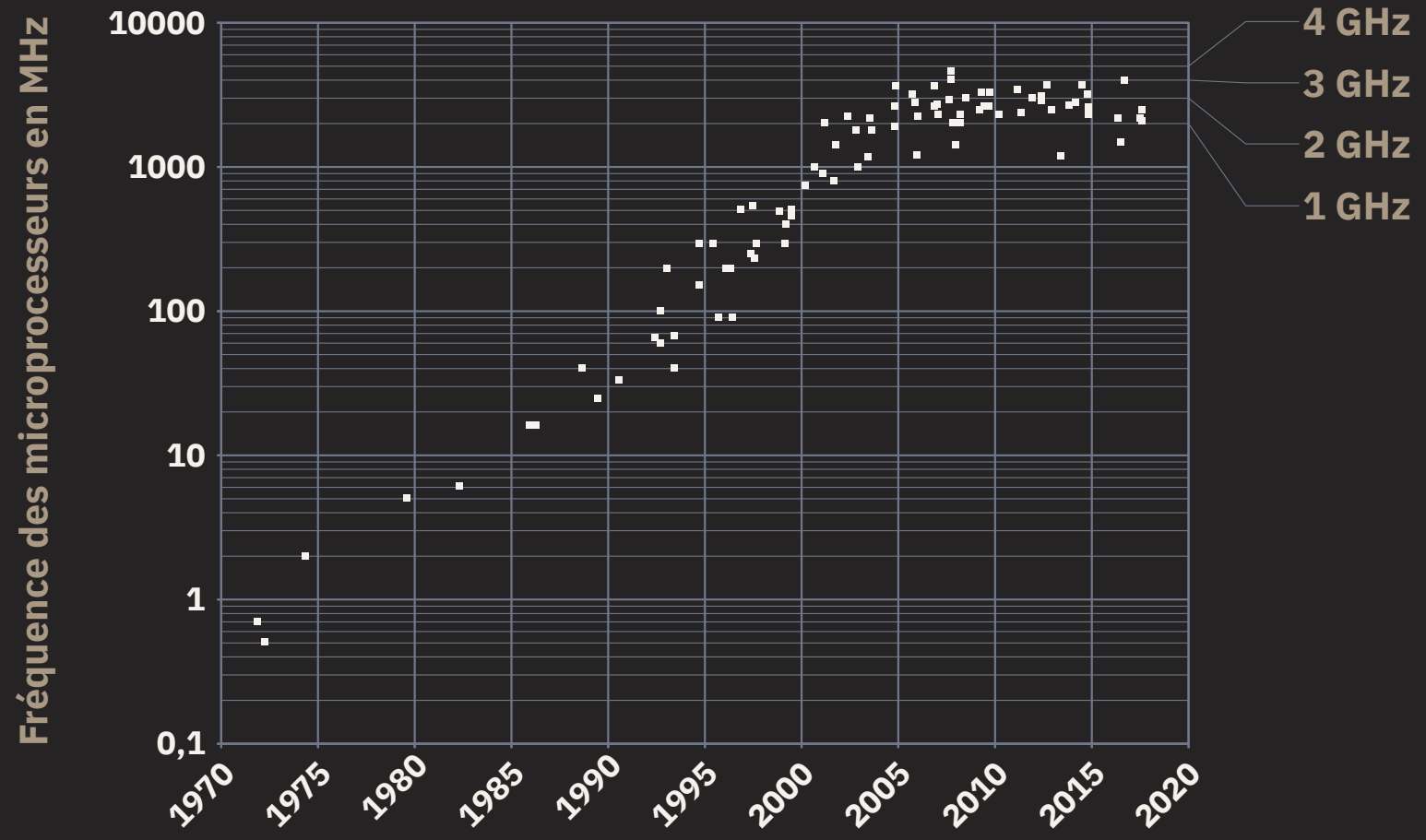
ÉVITONS LES PROCESSEURS PASSE-PLAT !



SOULAGEONS LE BUS DE DONNÉES

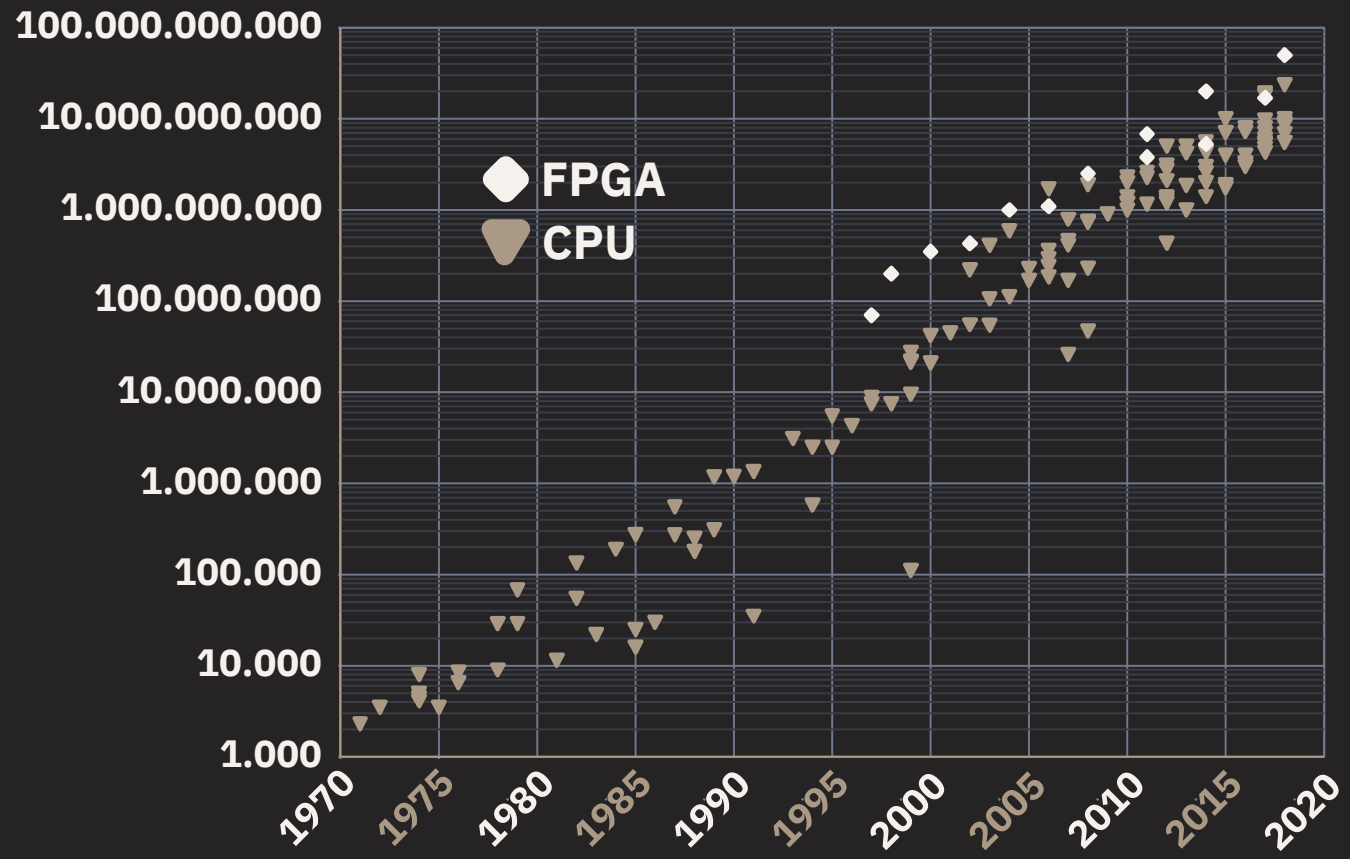


ACCÉLÉRER UNE 2CV N'EN FAIT PAS UNE FUSÉE



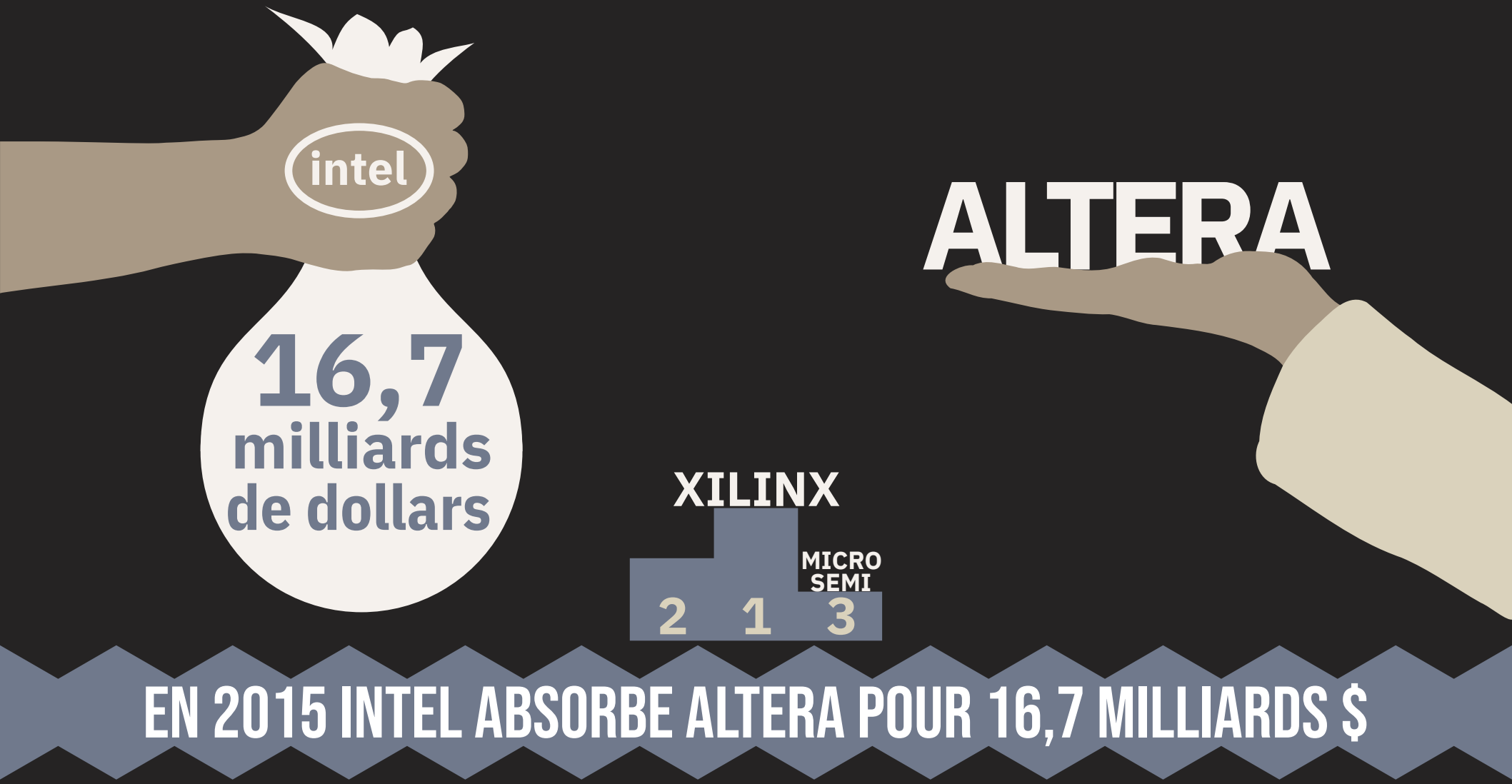
LES FRÉQUENCES STAGNENT DEPUIS 2005

Source: Karl Rupp, microprocessor trend data
Creative Commons Attribution 4.0 International Public License, 15/02/2018
https://github.com/karlrupp/microprocessor-trend-data

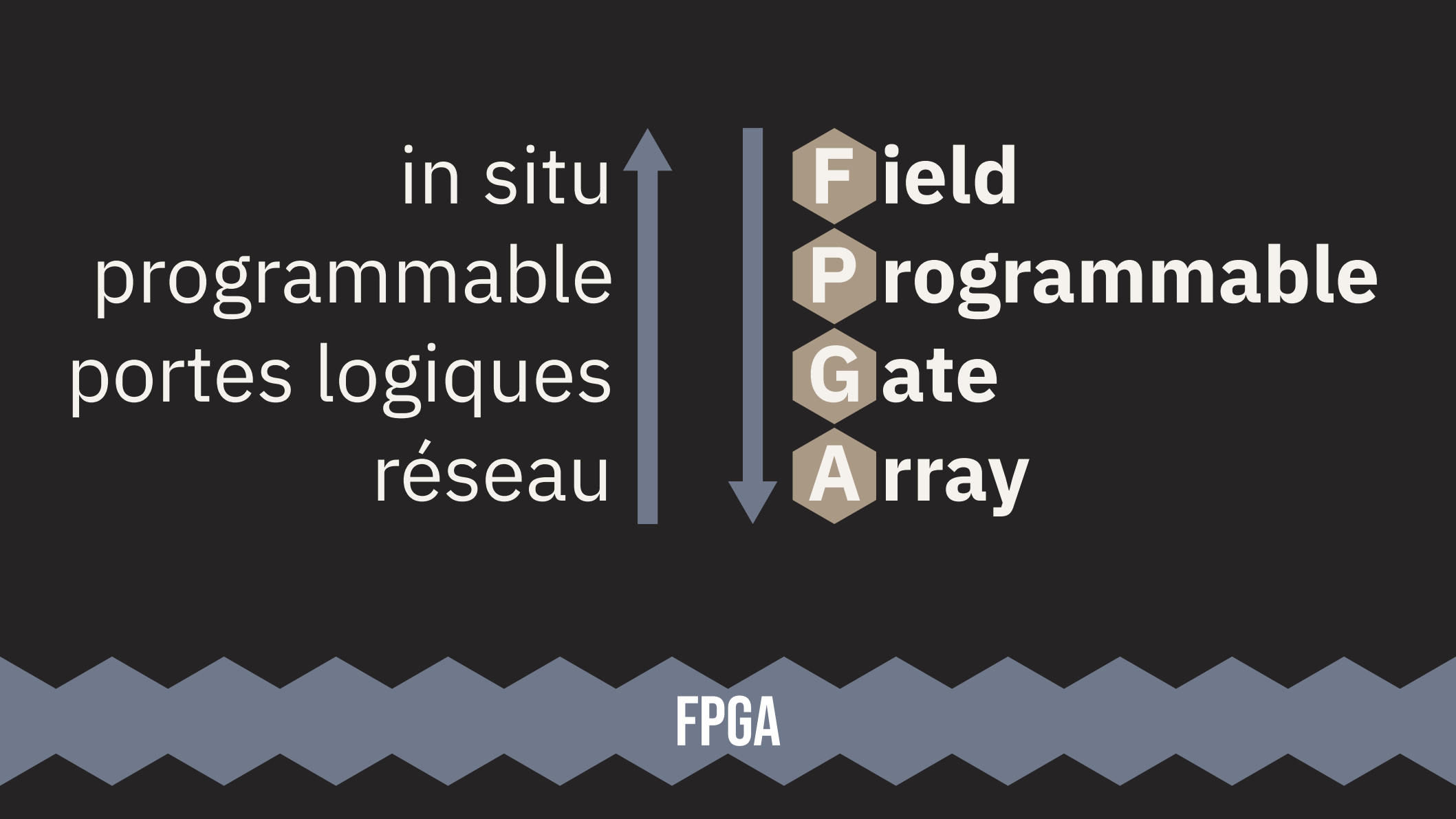


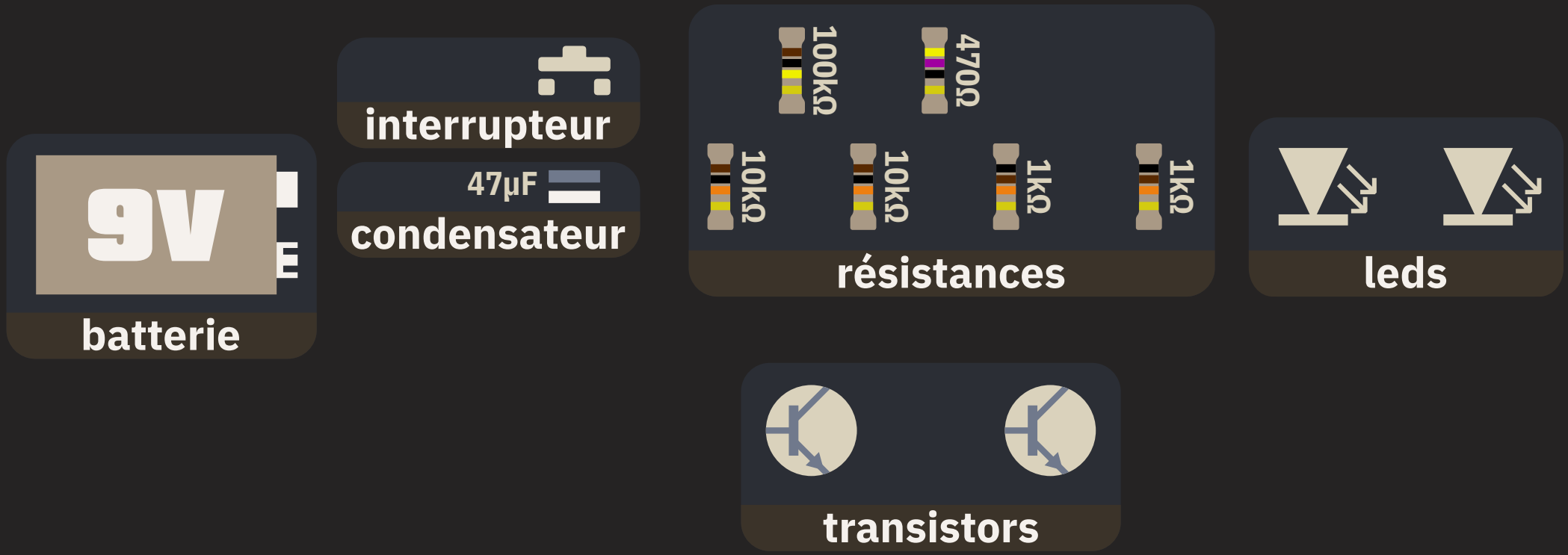
Source: Transistor count, 30/05/2019
https://en.wikipedia.org/wiki/Transistor_count

LA LOI DE MOORE A PERDURÉ JUSQU'EN 2017

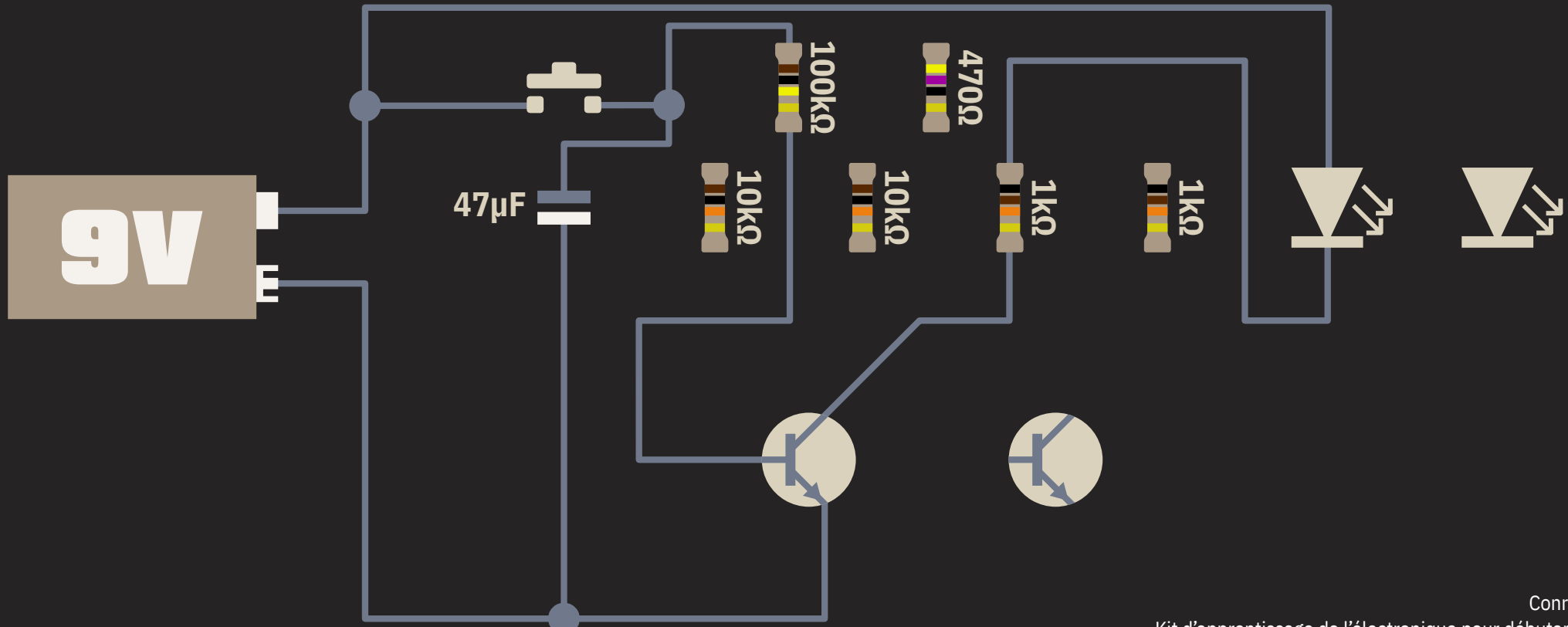

intel
16,7
milliards
de dollars
ALTERA
XILINX
MICRO
SEMI
2
1
3
EN 2015 INTEL ABSORBE ALTERA POUR 16,7 MILLIARDS $

C’EST QUOI UN FPGA ?


in situ
programmable
portes logiques
réseau
Field
Programmable
Gate
Array
FPGA

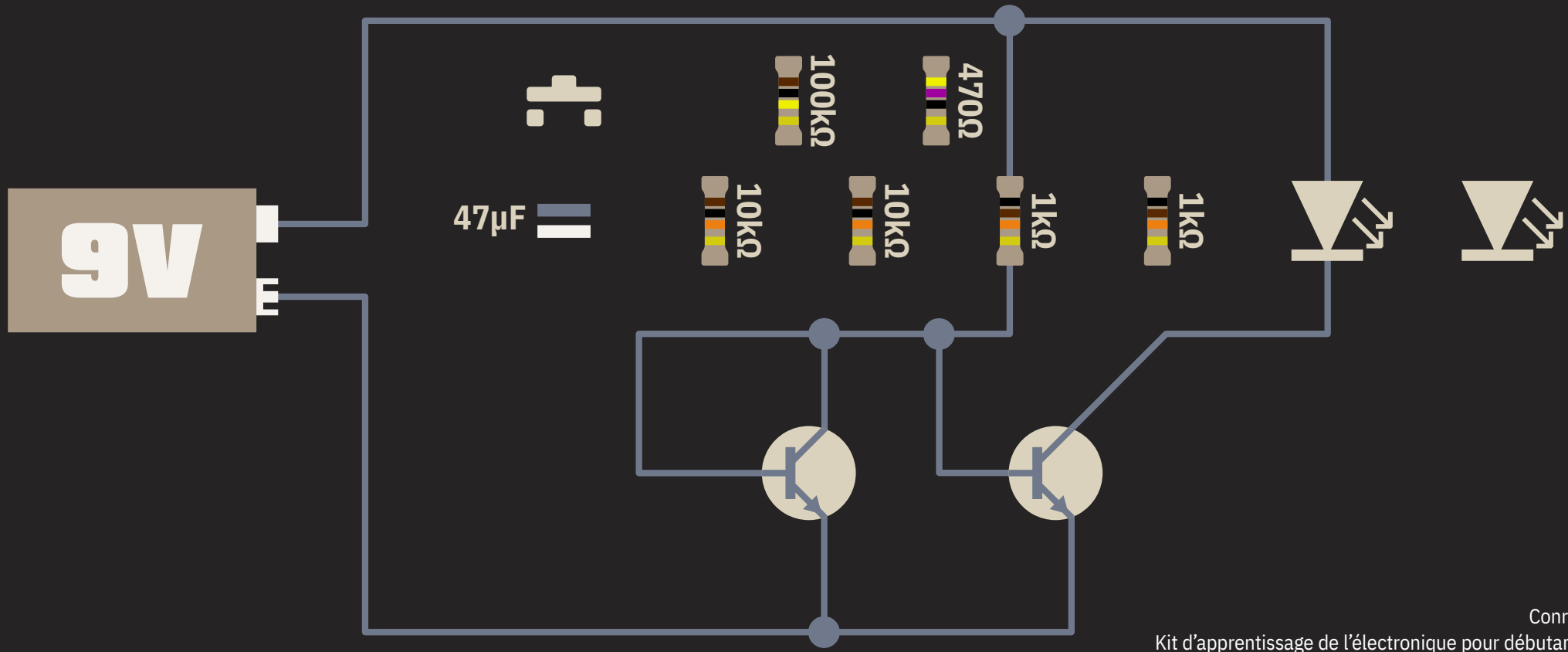


IMAGINEZ DES COMPOSANTS ÉLECTRONIQUES



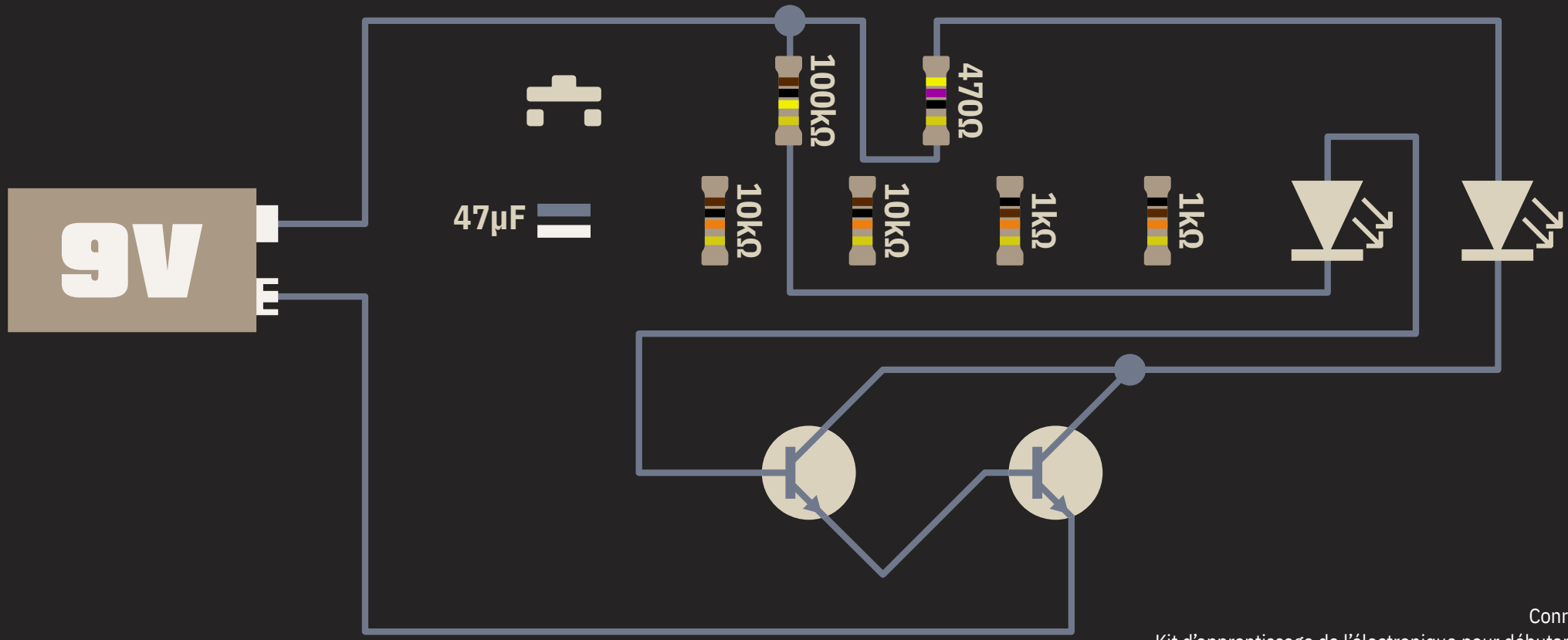
Conrad
Kit d'apprentissage de l'électronique pour débutants
https://produktinfo.conrad.com/datenblaetter/175000-199999/192230-an-01-fr-LERNPAKET_25_ELEKTRONIK_EXPERIMENTE.pdf

ILS PEUVENT FORMER UN RETARDATEUR



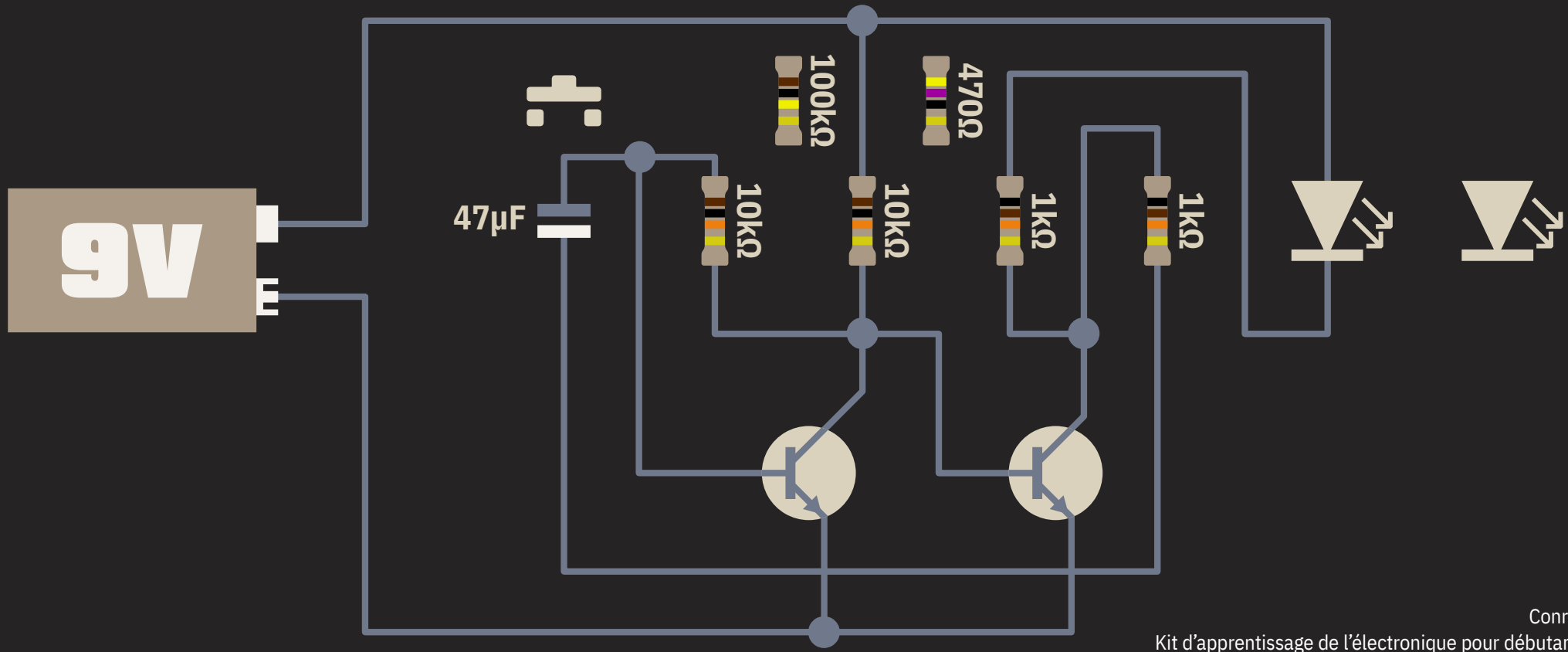
Conrad
Kit d'apprentissage de l'électronique pour débutants
https://produktinfo.conrad.com/datenblaetter/175000-199999/192230-an-01-fr-LERNPAKET_25_ELEKTRONIK_EXPERIMENTE.pdf

UN CAPTEUR DE TEMPÉRATURE



Conrad
Kit d'apprentissage de l'électronique pour débutants
https://produktinfo.conrad.com/datenblaetter/175000-199999/192230-an-01-fr-LERNPAKET_25_ELEKTRONIK_EXPERIMENTE.pdf

UN CAPTEUR DE LUMIÈRE



Conrad
Kit d'apprentissage de l'électronique pour débutants
https://produktinfo.conrad.com/datenblaetter/175000-199999/192230-an-01-fr-LERNPAKET_25_ELEKTRONIK_EXPERIMENTE.pdf

OU ENCORE UNE LED CLIGNOTANTE

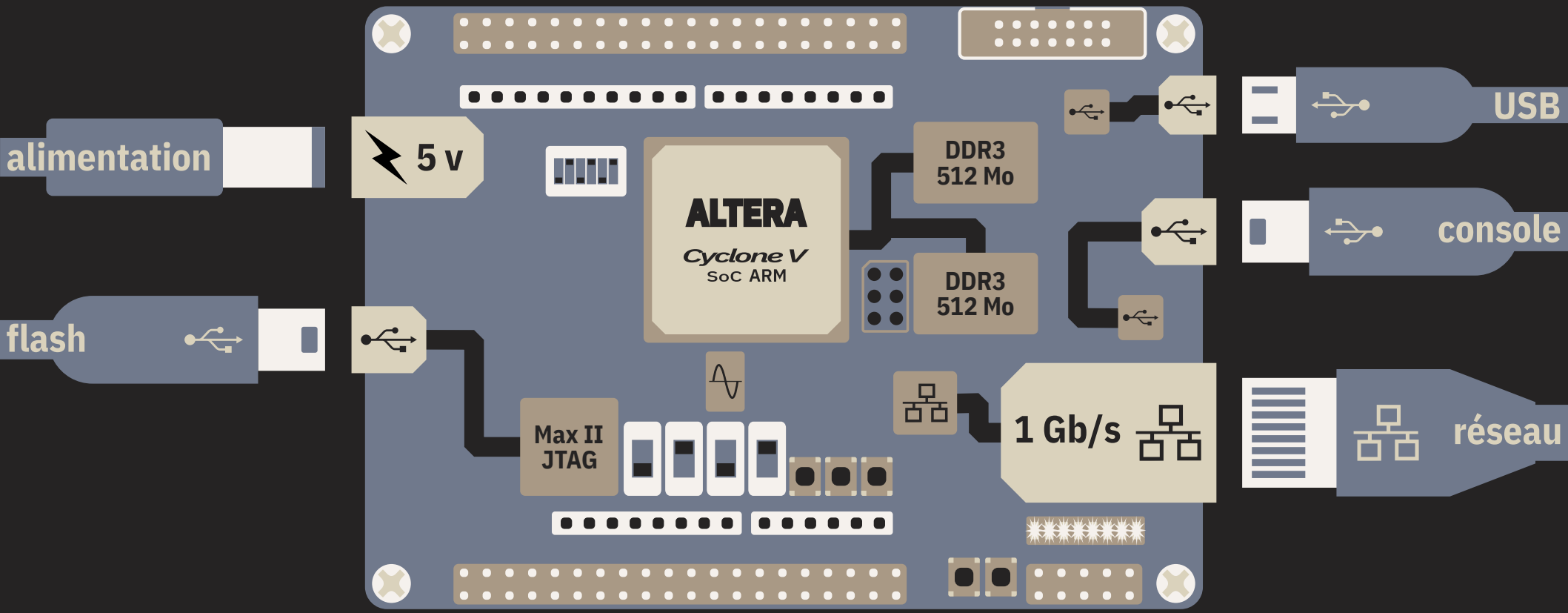
QUELQUES REMARQUES

- Le câblage définit le fonctionnement du circuit
- Les composants
  - restent fixes entre les différents schémas
  - ne sont pas tous utilisés pour un schéma donné
- C’est le principe d’un FPGA !

Réseau de portes logiques programmable in situ

- Un FPGA a 3 éléments constitutifs
  - des élément logiques (ALM/CLB, mémoire, DSP...)
  - un réseau de pistes
  - une mémoire de configuration
- Le réseau de pistes est figé
  - un FPGA reste un circuit intégré
  - toutes les combinaisons ne sont pas possibles
  - il est reconfigurable à volonté grâce à la mémoire

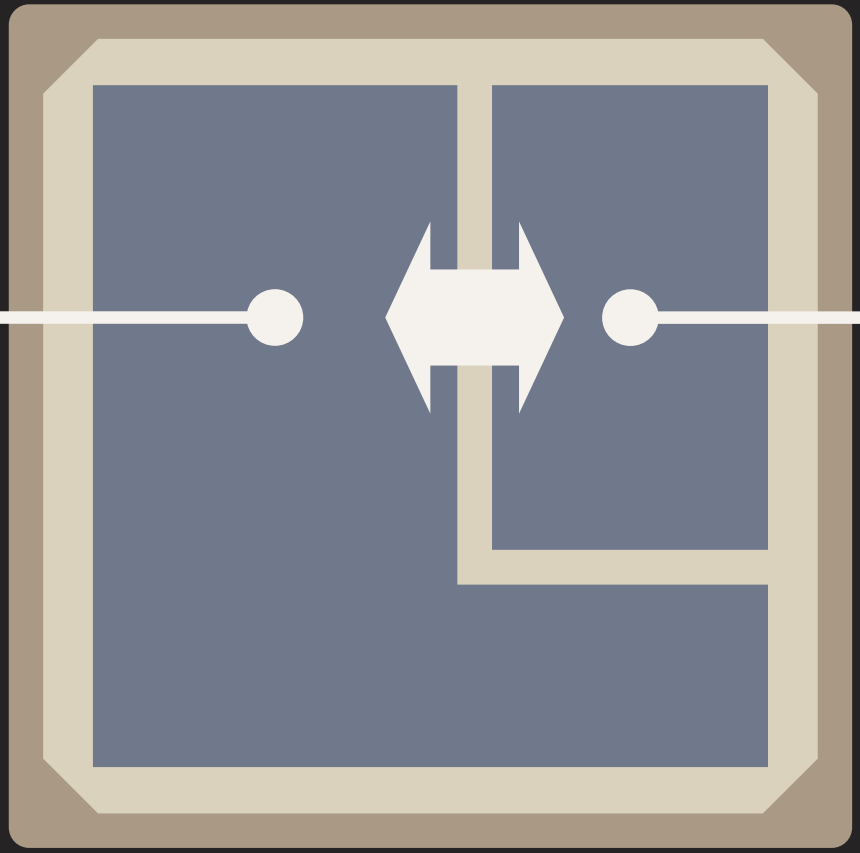
LE DEO-NANO-SOC



LA PLATEFORME D'INITIATION DE0-NANO-SOC

FPGA

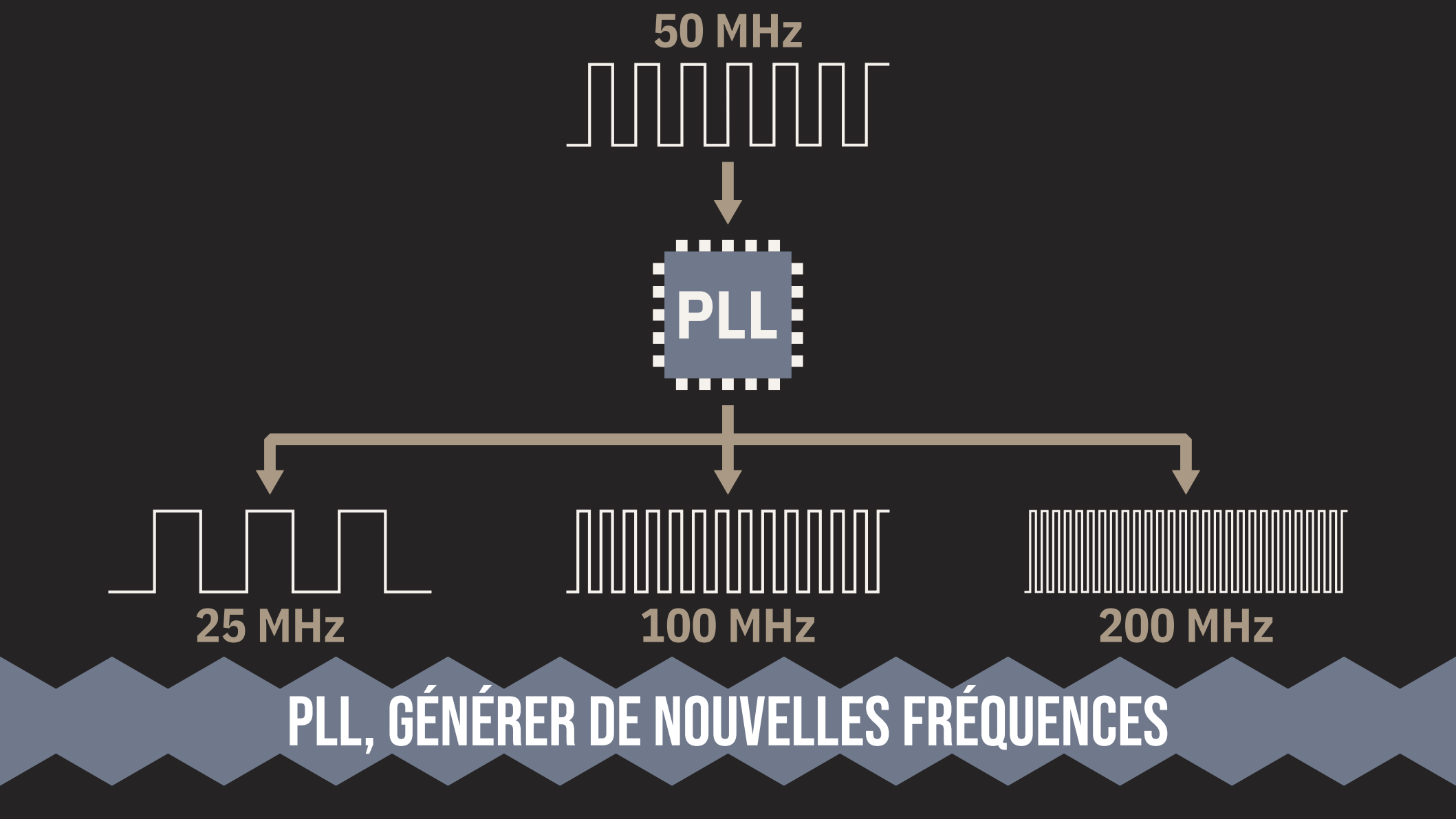
15880 CLB
330 Ko RAM
50 MHz



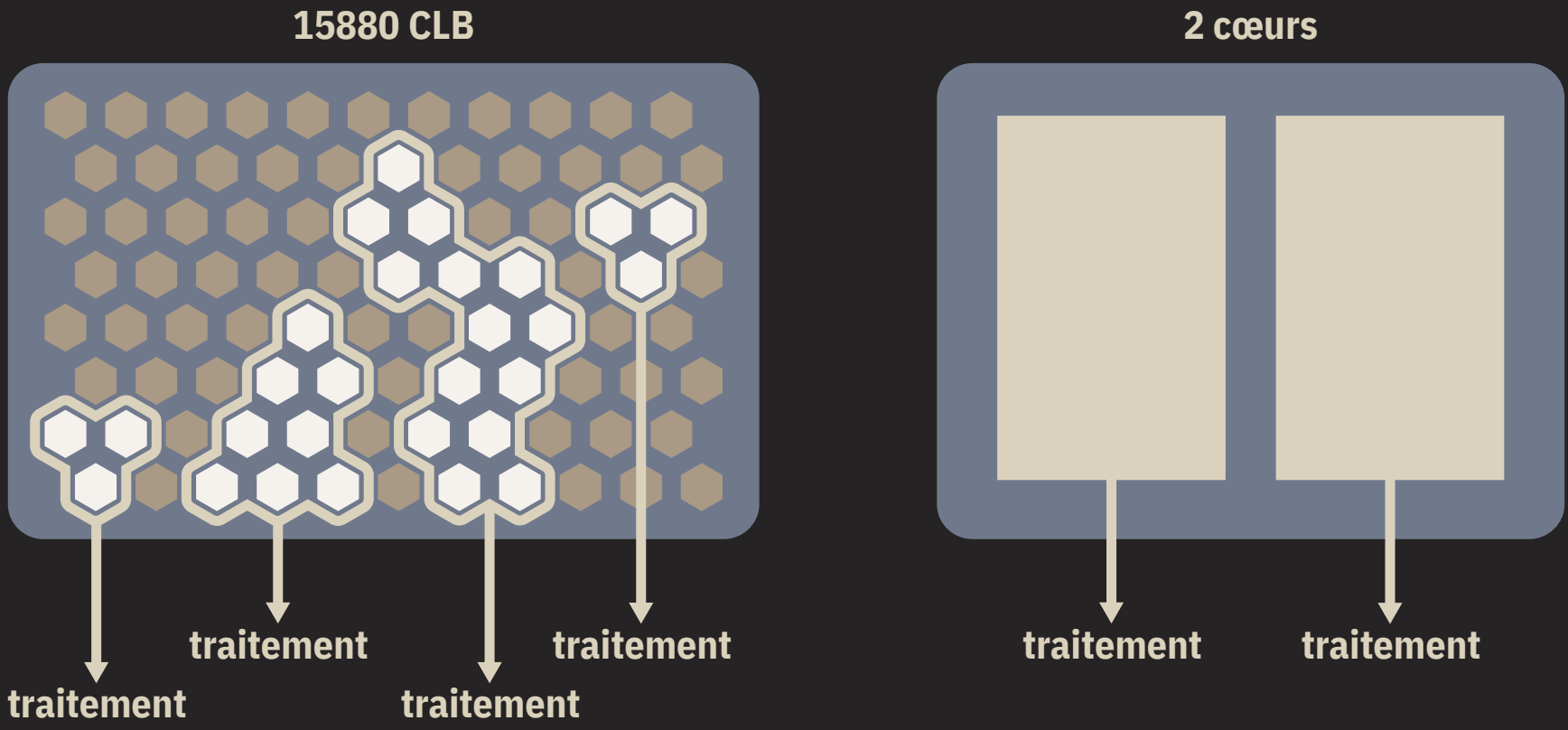
ARM Cortex-A9

2 cœurs
925 MHz

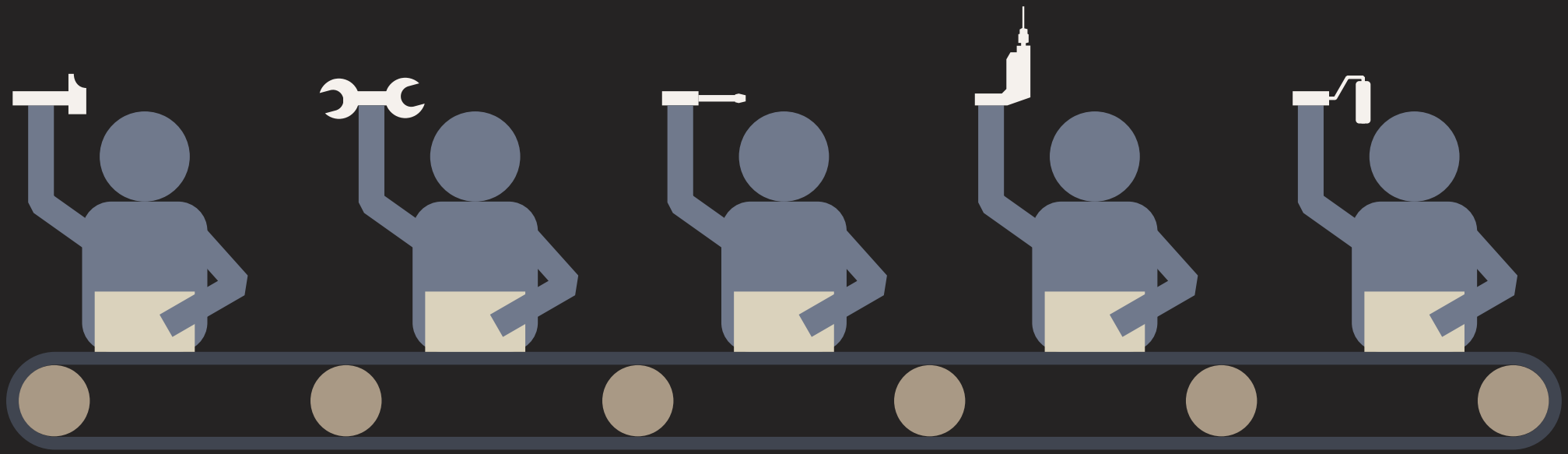
AU CŒUR DU DE0-NANO-SOC : LE CYCLONE V



PLL, GÉNÉRER DE NOUVELLES FRÉQUENCES



MODULAIRE ET EXTRÊMEMENT PARALLÈLE



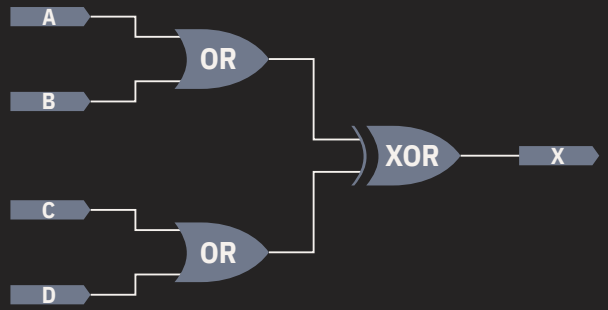
PIPELINE, TRAVAIL À LA CHAÎNE

COMMENT PROGRAMMER UN FPGA ?

LES OUTILS DISPONIBLES

- Chaque fabricant a ses propres outils
  - Xilinx → Vivado/ISE
  - Intel → Quartus Prime
  - Lattice → Diamond
  - etc.
- Ils sont **indispensables** pour générer l'image bitstream
  - ils sont gratuits pour les cartes d'initiation
  - les outils libres ne couvrent pas tout le flot de conception

dessiner un schéma



avec des portes logiques,
des composants électroniques

utiliser un HDL ou langage de description de matériel

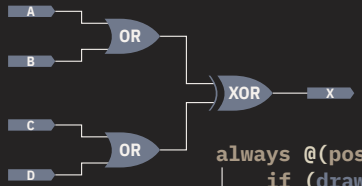
```
always @(posedge clk) begin
    if (draw) begin
        pixel <= 1'b1;
    end else begin
        pixel <= 1'b0;
    end
end
```

pour décrire le comportement
du circuit souhaité

utiliser OpenCL

pour utiliser un langage
de haut niveau

3 FAÇONS DE PROGRAMMER UN FPGA




```
always @(posedge clk) begin
    if (draw) begin
        pixel <= 1'b1;
    end else begin
        pixel <= 1'b0;
    end
end
```

simulation débogage

HDL

analyse synthèse

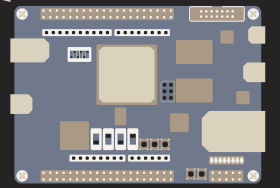
netlist

placement routage

assembleur

assemblage

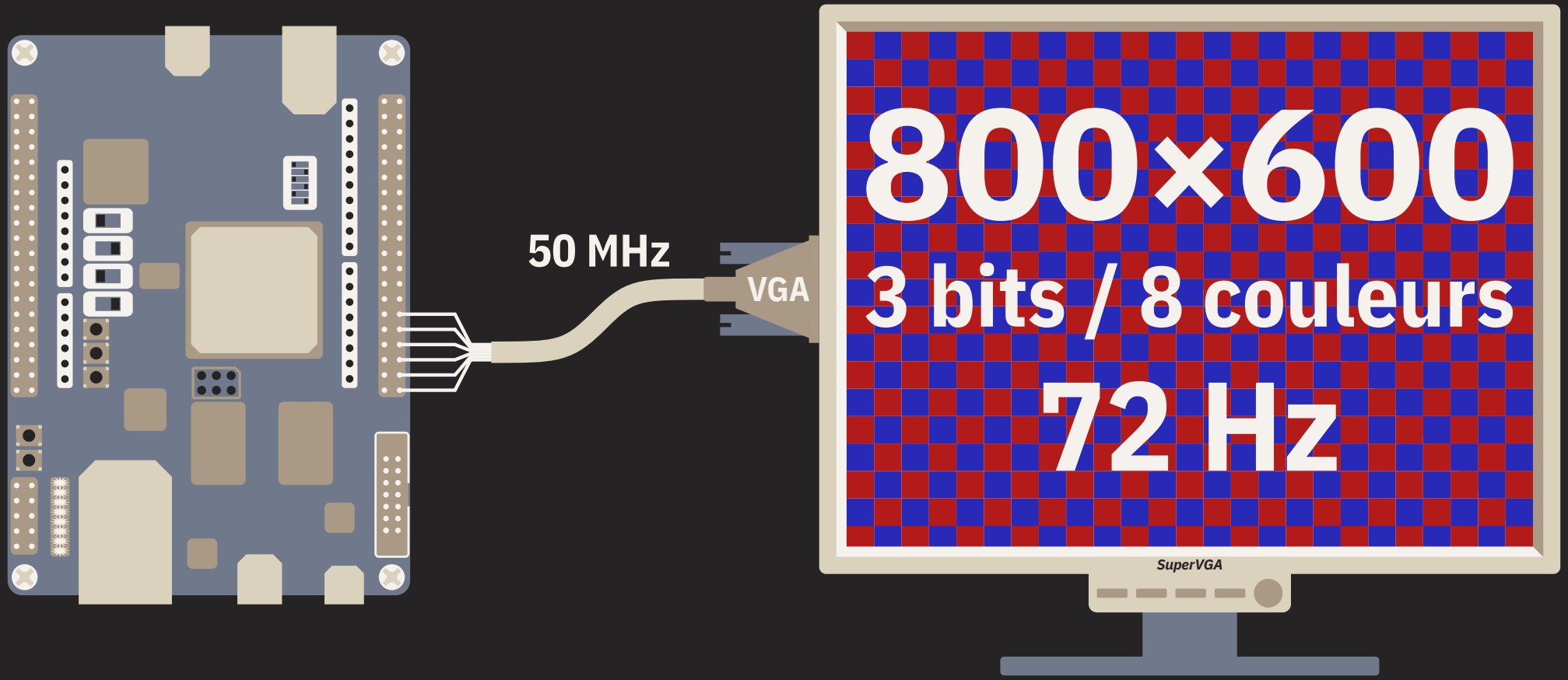
bitstream



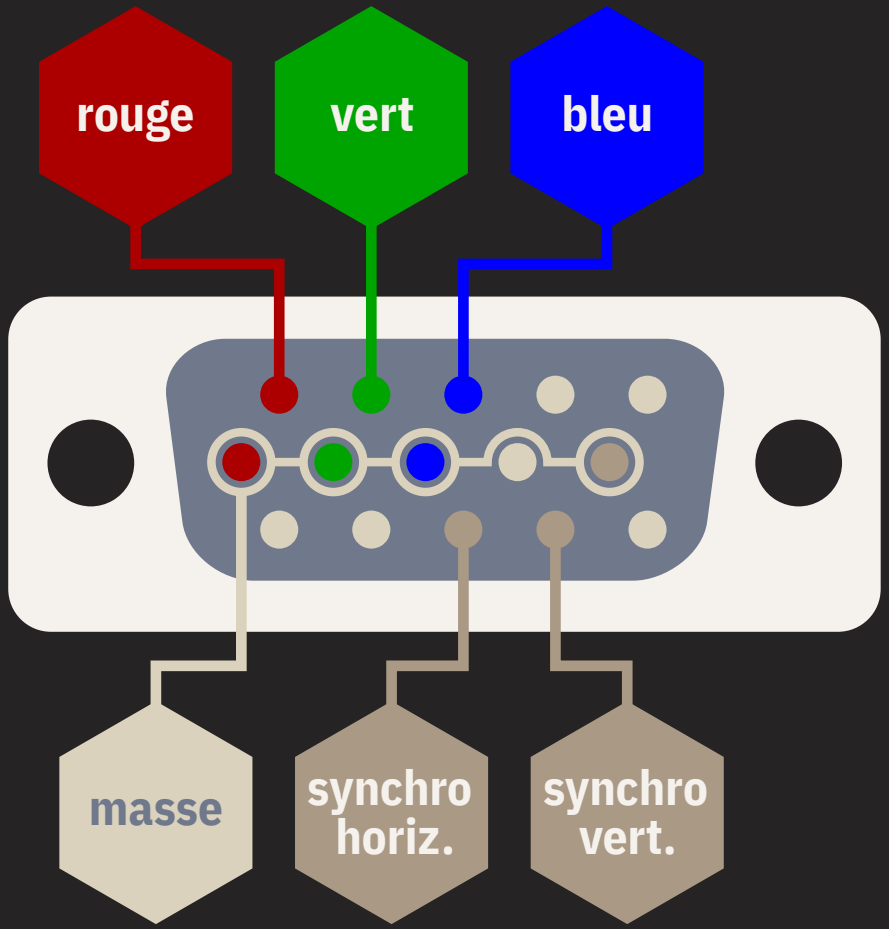
de quelques minutes à plusieurs heures !

LE FLOT DE CONCEPTION

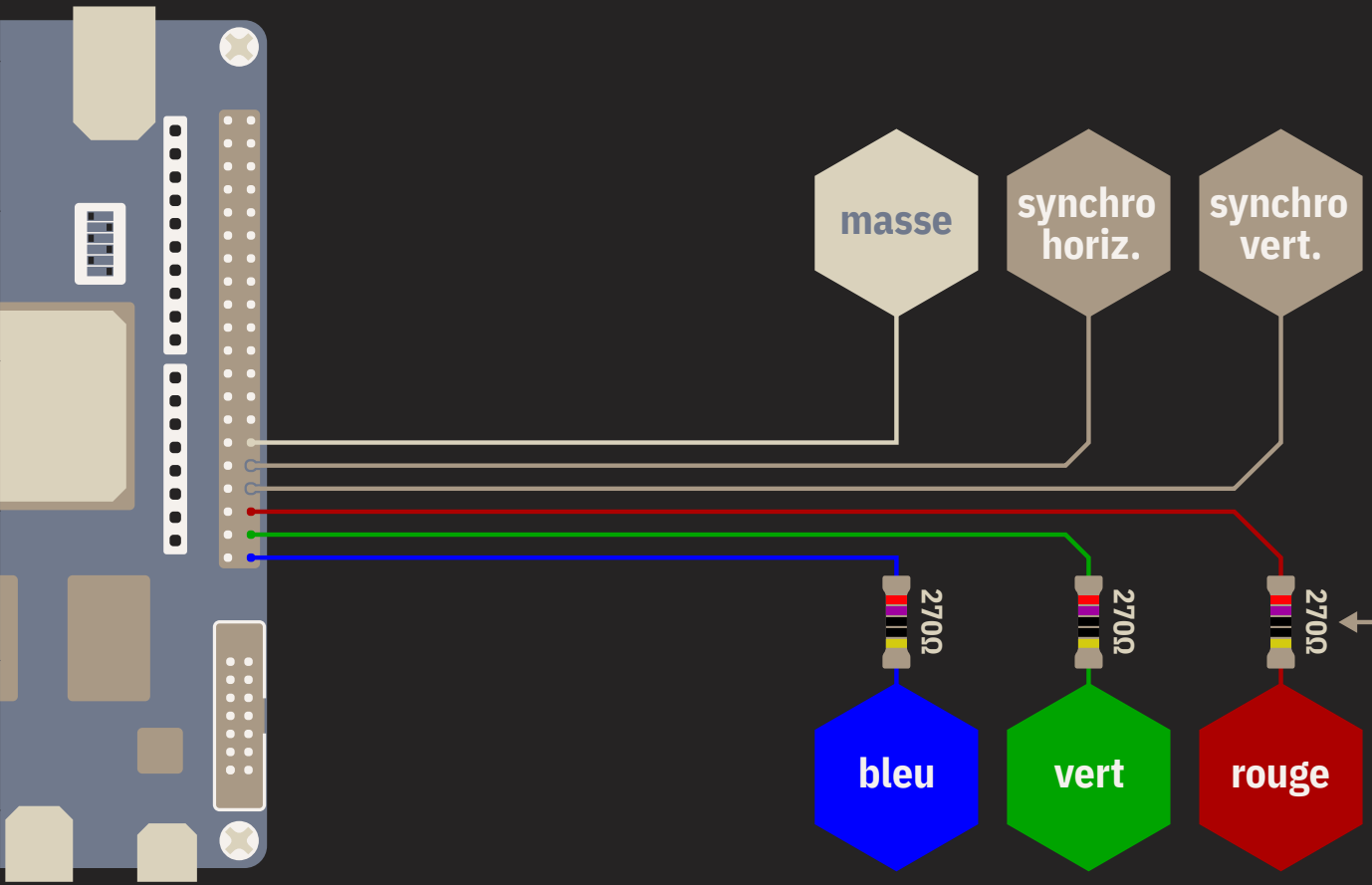
UN EXEMPLE : SIMPLEVGA



GÉNÉRATION D'UN SIGNAL VIDÉO VGA



LA PRISE VGA

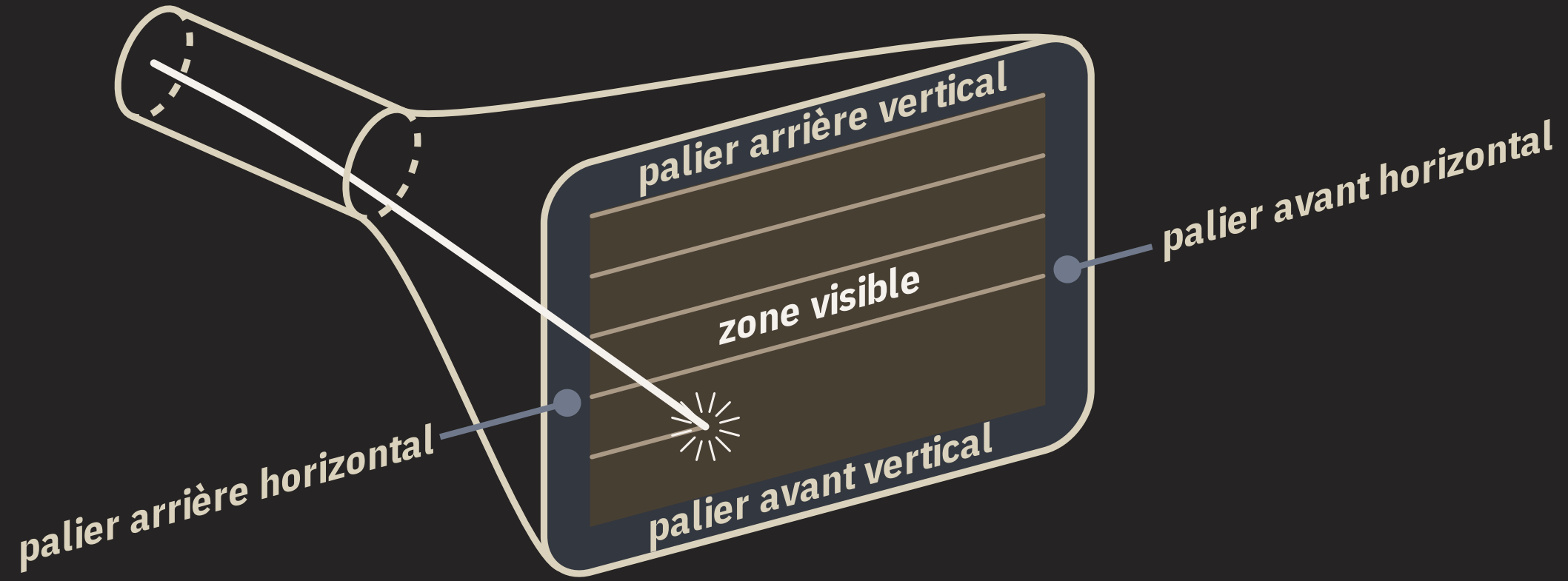


les broches du DE0-Nano-SoC utilisent une tension de 3,3 volts

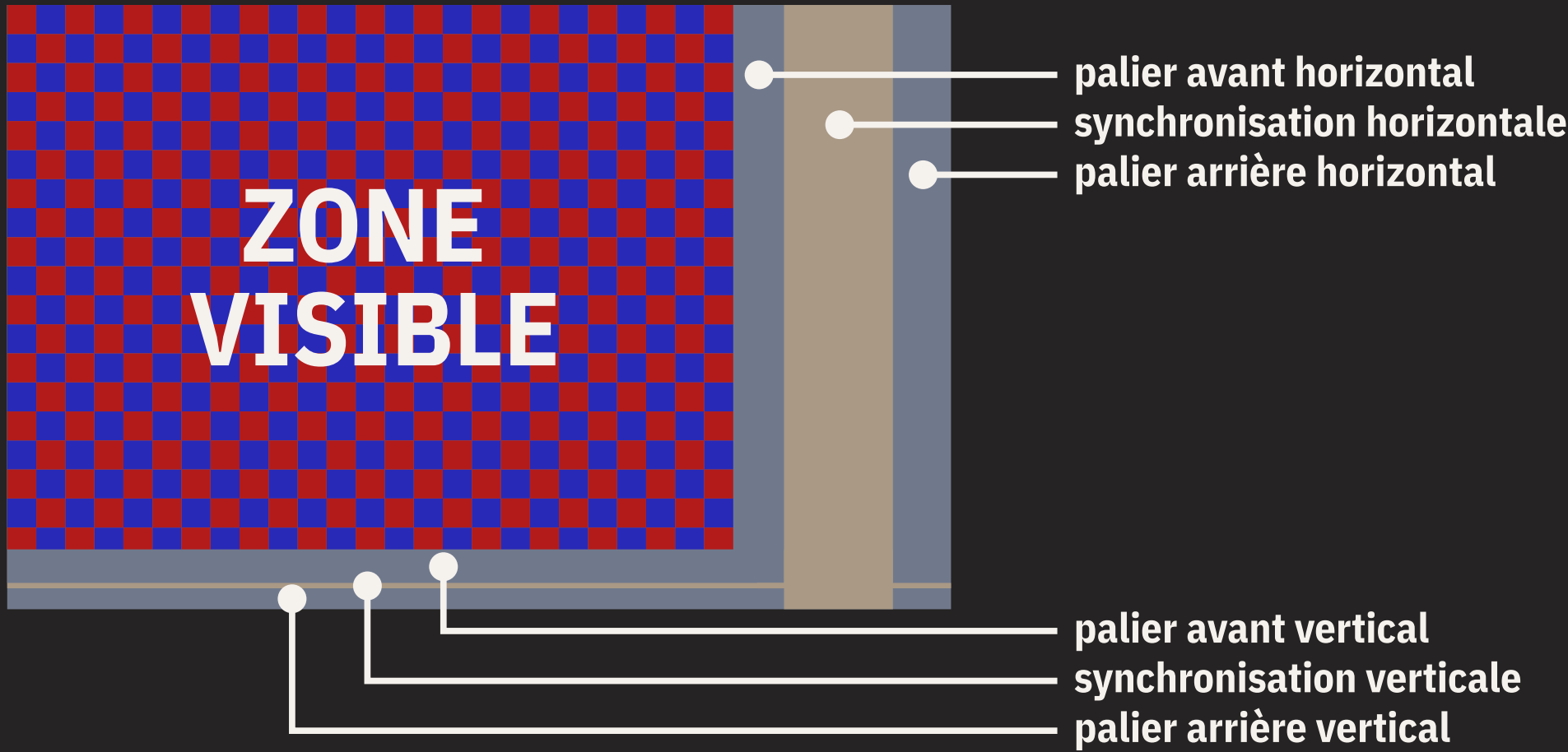
l'intensité lumineuse maximum est de 0,7 volts en VGA

les résistances permettent d'adapter la tension

CONNECTER LA PRISE VGA AU DE0-NANO-SOC



UN SIGNAL VIDÉO HÉRITÉ DES TUBES CATHODIQUES



LE SIGNAL VGA

ÉCRITURE DU CODE VERILOG

1) Déclaration du module
2) Synchronisation horizontale
3) Synchronisation verticale
4) Damier rouge et bleu

1

```
module SimpleVGA (
        input wire clk,

        output wire hsync,
        output wire vsync,
        output reg red,
        output reg green,
        output reg blue
);
```

2

```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```

3

```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```

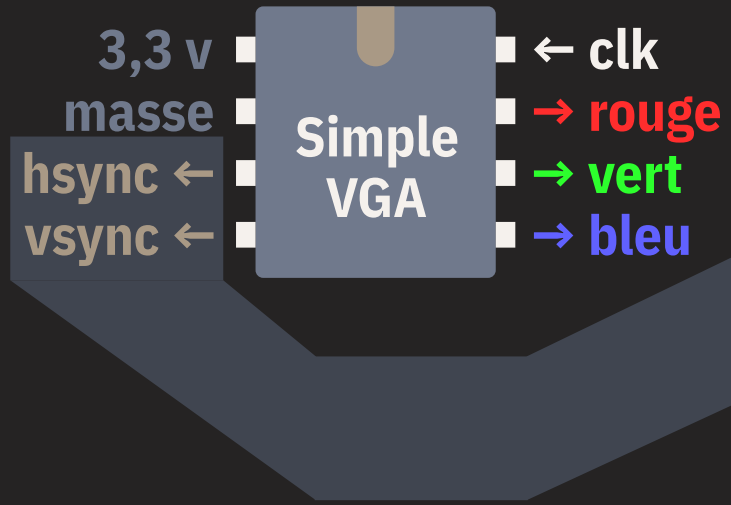
4

```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end

endmodule
```

DÉCLARATION DU MODULE


```
module SimpleVGA (
    input  wire clk,

    output wire hsync,
    output wire vsync,
    output reg  red,
    output reg  green,
    output reg  blue
);
```

CRÉATION DU CIRCUIT INTÉGRÉ, HORLOGE



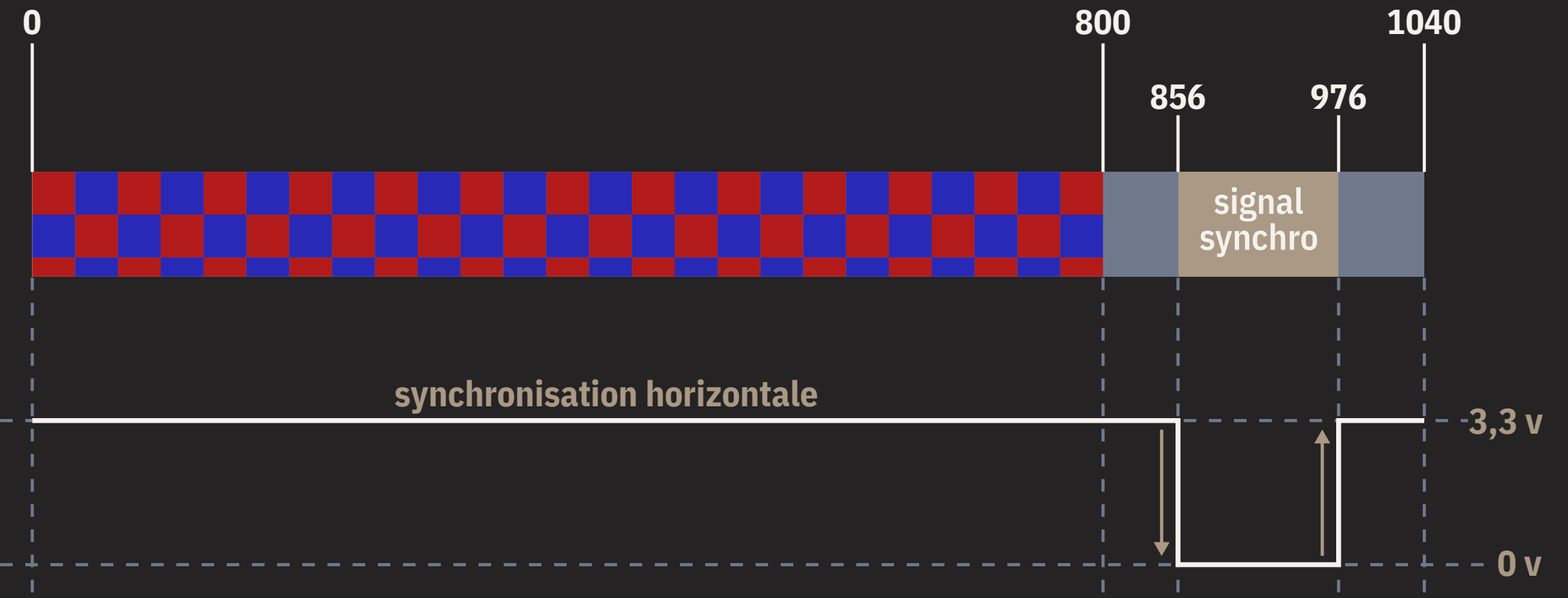

```
module SimpleVGA (
        input  wire clk,

        output wire hsync,
        output wire vsync,
        output reg  red,
        output reg  green,
        output reg  blue
);
```

CRÉATION DU CIRCUIT INTÉGRÉ, SYNCHRONISATION


```
module SimpleVGA (
        input  wire clk,

        output wire hsync,
        output wire vsync,
        output reg  red,
        output reg  green,
        output reg  blue
);
```

CRÉATION DU CIRCUIT INTÉGRÉ, COULEURS

SYNCHRONISATION HORIZONTALE



DÉCLENCHEMENT DE LA SYNCHRONISATION HORIZONTALE

```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```

CODE GÉNÉRANT LA SYNCHRONISATION HORIZONTALE

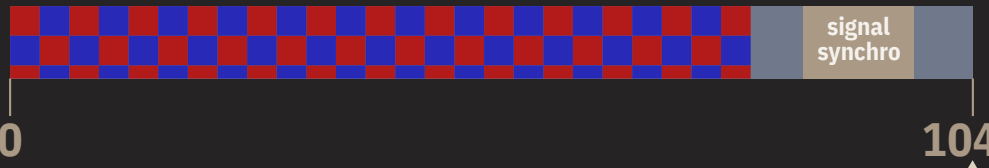
registre de 11 bits = valeurs de 0 à 2047

```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```

DÉCLARATION D'UN REGISTRE DE 11 BITS


```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```

EXÉCUTION À CHAQUE FRONT MONTANT




```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```

REMISE À ZÉRO APRÈS 1040 POINTS

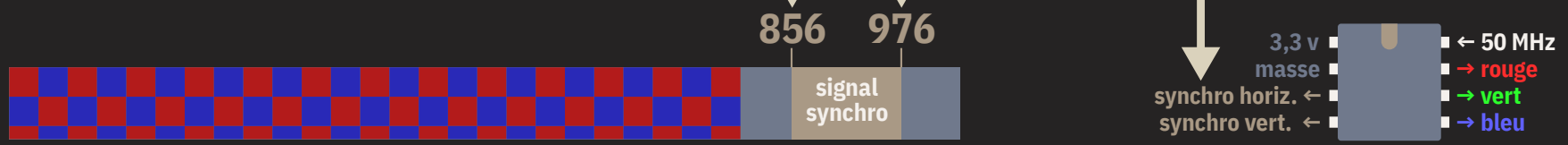

```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```

COMPTAGE DE 0 À 1039

exécution continue

exécution rythmée par une horloge

```
reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;
```



GÉNÉRATION DE LA SYNCHRONISATION HORIZONTALE

SYNCHRONISATION VERTICALE

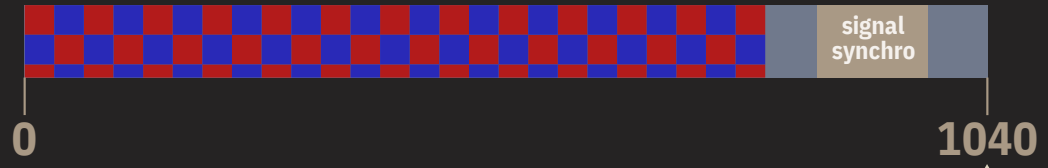
```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```

CODE GÉNÉRANT LA SYNCHRONISATION VERTICALE

registre de 10 bits = valeurs de 0 à 1023

```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```

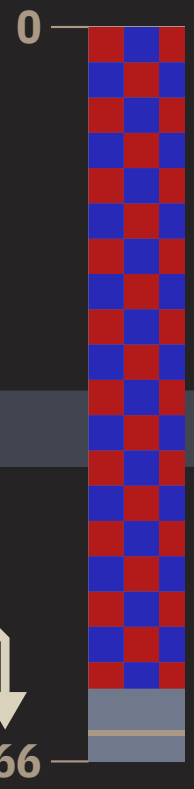
DÉCLARATION D'UN REGISTRE DE 10 BITS




```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```

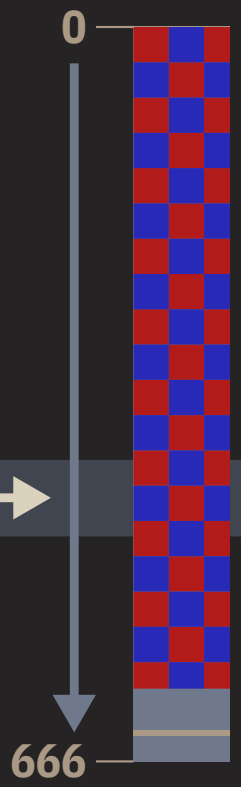
CALCUL À CHAQUE FIN DE LIGNE

```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```



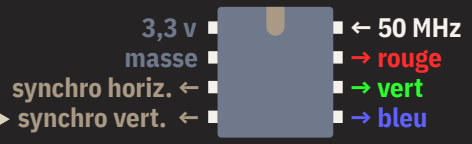
REMISE À ZÉRO APRÈS 666 LIGNES

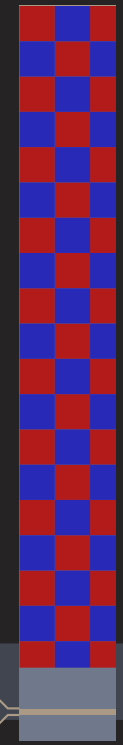
```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```



COMPTAGE DE 0 À 665

```
reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039) begin
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;
        end

assign vsync = ypos < 637 || ypos >= 643;
```





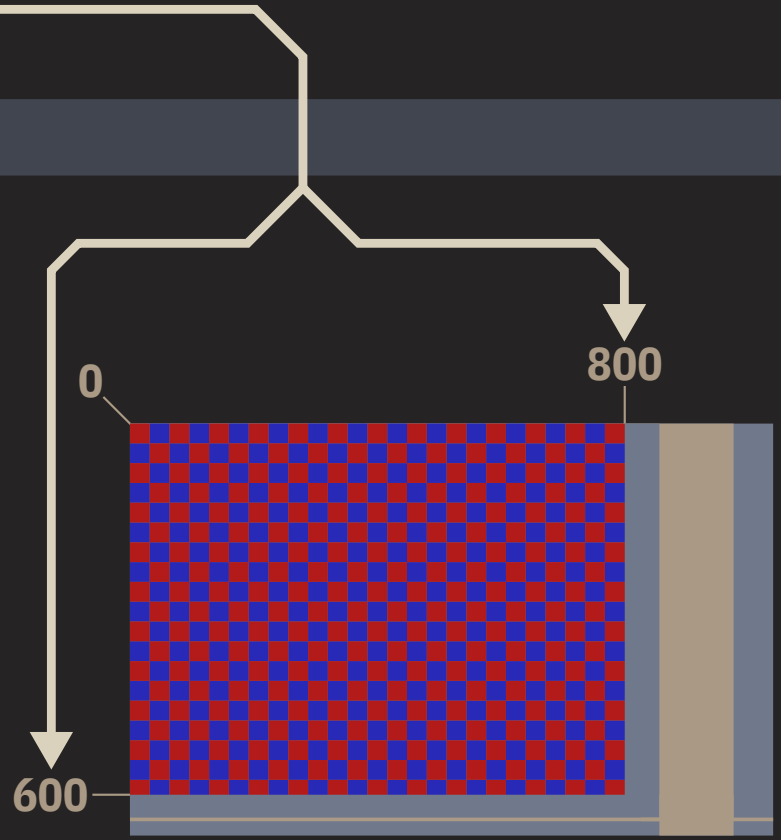
GÉNÉRATION DE LA SYNCHRONISATION VERTICALE

DAMIER ROUGE ET BLEU

```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```

CODE GÉNÉRANT LE DAMIER ROUGE ET BLEU

```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```



TEST DE LA ZONE VISIBLE

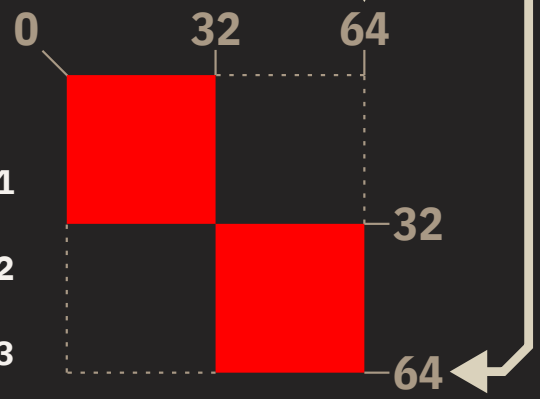
```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```

les 3 calculs et affectations sont exécutés en parallèle

UN FPGA TRAVAILLE EN PARALLÈLE

```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```

10	9	8	7	6	**5**	4	3	2	1	0	
0	0	0	0	0	**0**	0	0	0	0	0	= 0
0	0	0	0	0	**0**	1	1	1	1	1	= 31
0	0	0	0	0	**1**	0	0	0	0	0	= 32
0	0	0	0	0	**1**	1	1	1	1	1	= 63

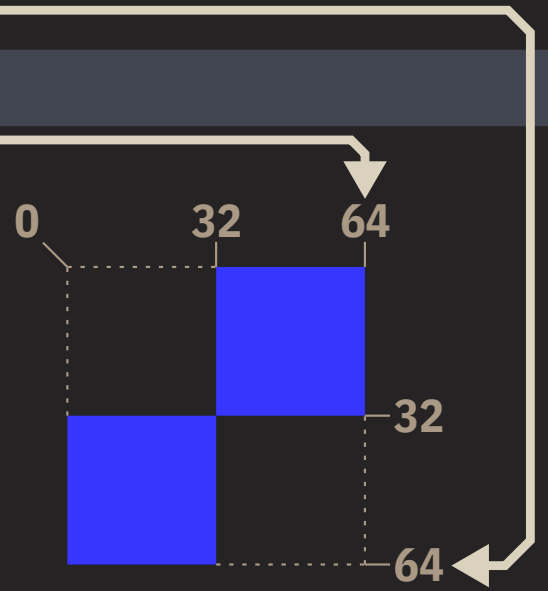


ALTERNER LES CARRÉS ROUGES

```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```

LE VERT N'EST JAMAIS UTILISÉ

```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```



ALTERNER LES CARRÉS BLEUS

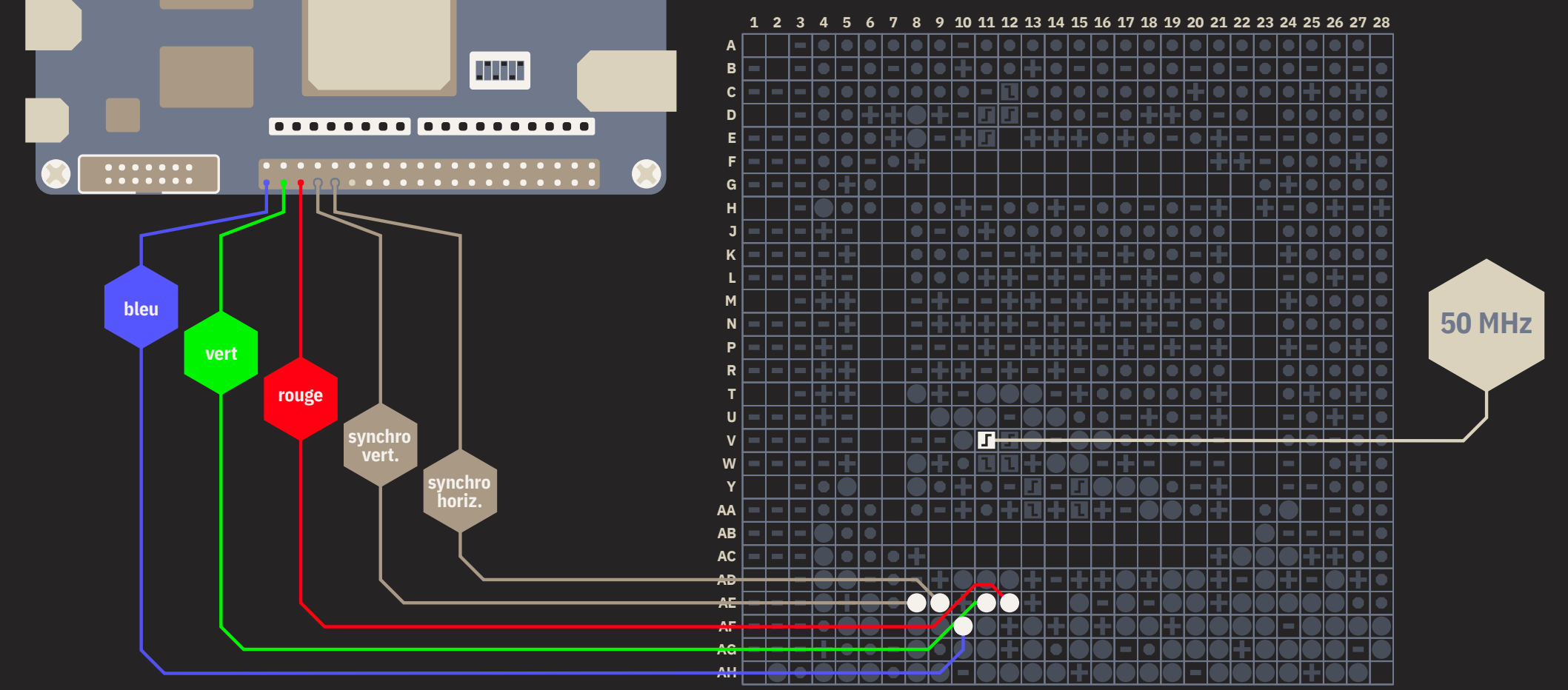
```
always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red   <= ~xpos[5] ^ ypos[5];
                green <= 0;
                blue  <=  xpos[5] ^ ypos[5];
        end else begin
                red   <= 0;
                green <= 0;
                blue  <= 0;
        end
```

AUCUNE COULEUR EN DEHORS DE LA ZONE VISIBLE

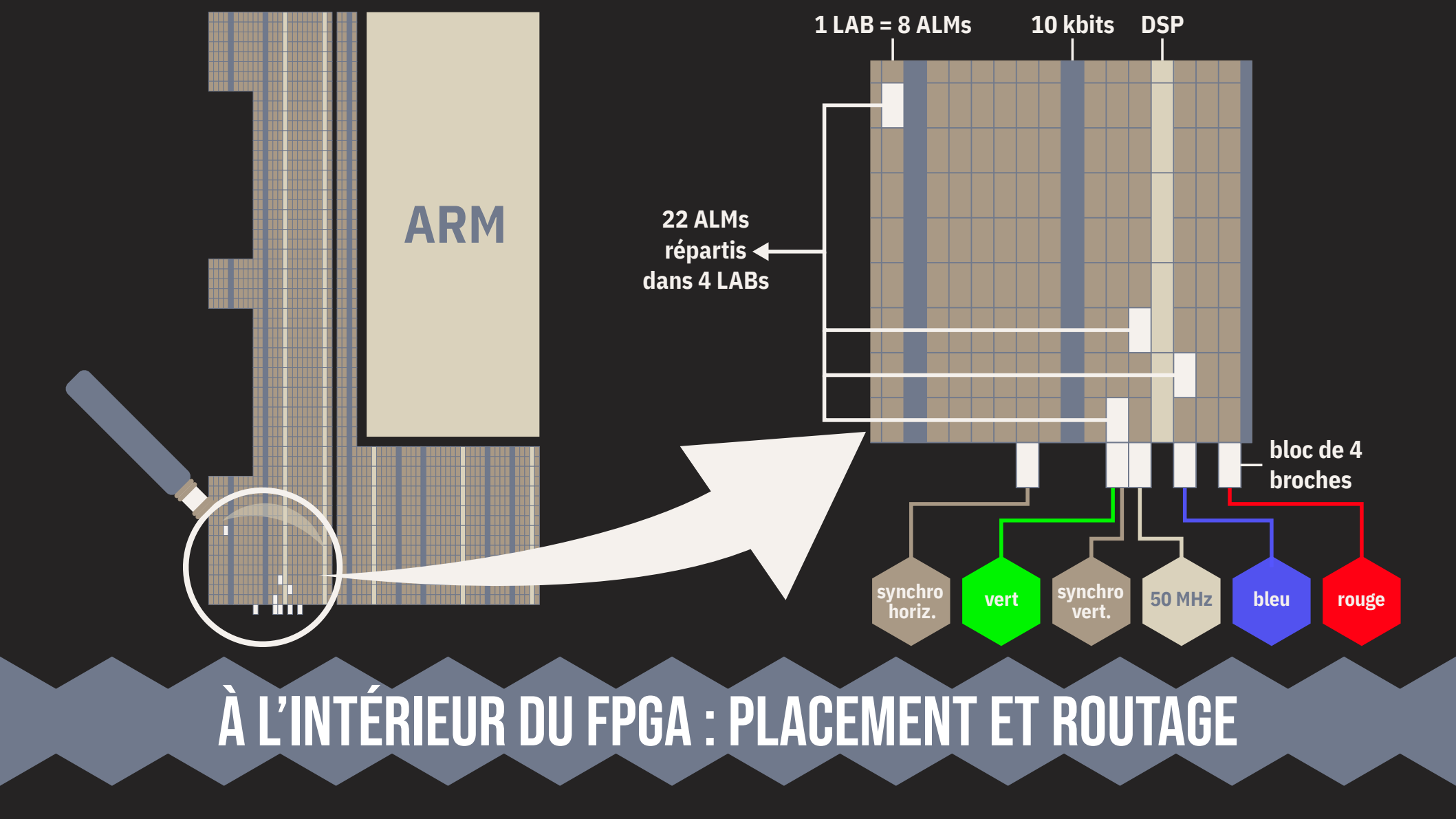
Remarques et pièges

- Verilog n’est **pas un langage procédural**
- Un bit peut avoir 4 états
  - 0, 1, X et Z → faux, vrai, inconnu, impédance haute
- Vous êtes responsables des délais de propagation
- Générer une image « bitstream » est long…
- Tous les codes HDL ne sont pas synthétisables

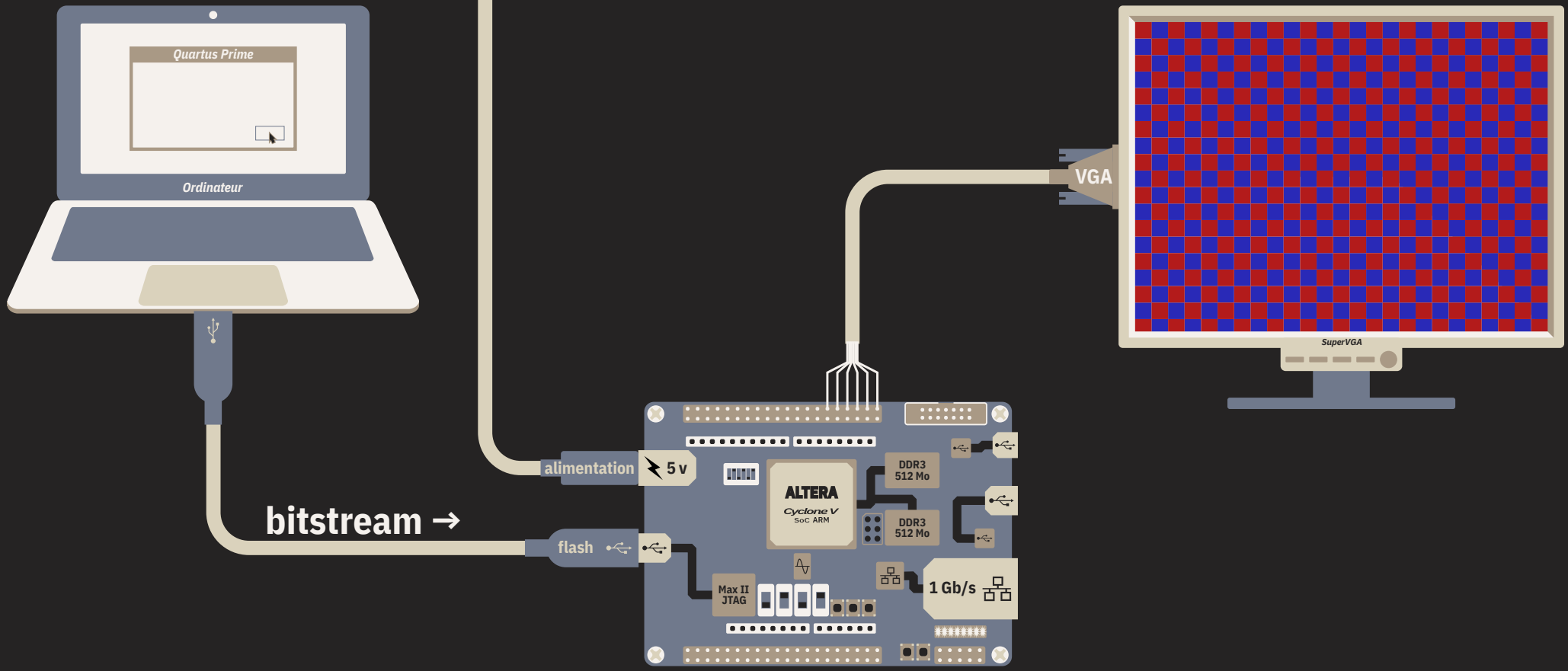
GÉNÉRATION DE L'IMAGE « BITSTREAM »



À L'EXTÉRIEUR DU FPGA : AFFECTATION DES BROCHES

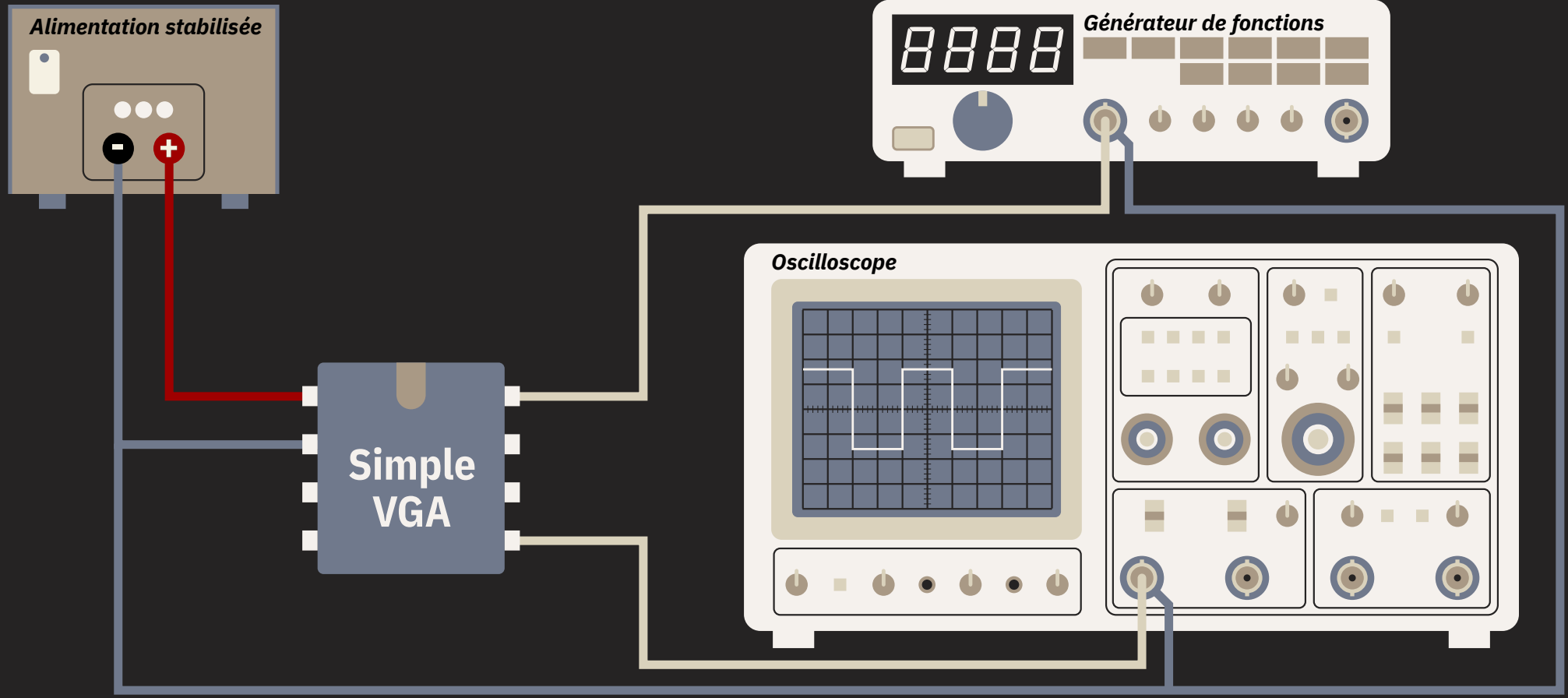


À L'INTÉRIEUR DU FPGA : PLACEMENT ET ROUTAGE



ENVOI DE L'IMAGE « BITSTREAM »

DÉBOGUER UN CIRCUIT



DÉBOGUER PHYSIQUEMENT

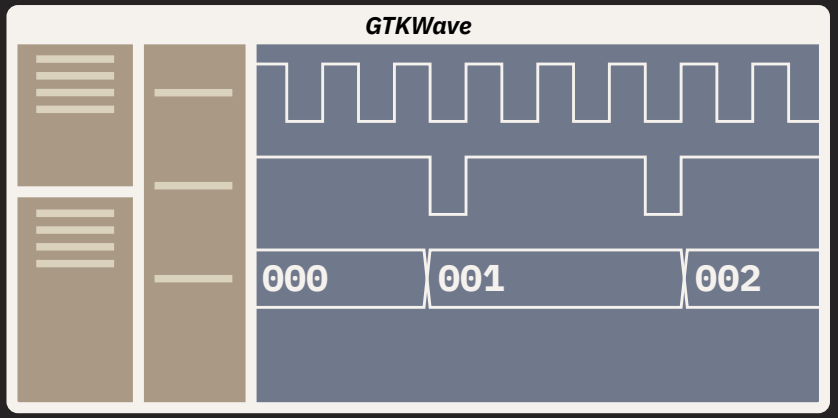
Icarus Verilog

```
module SimpleVGA (
        input wire clk,

        output wire hsync,
        output wire vsync,
        output reg red,
        output reg green,
        output reg blue
);

reg [10:0] xpos = 0;
always @(posedge clk)
        if (xpos == 1039) xpos <= 0;
        else              xpos <= xpos + 1;

assign hsync = xpos < 856 || xpos >= 976;

reg [9:0] ypos = 0;
always @(posedge clk)
        if (xpos == 1039)
                if (ypos == 665) ypos <= 0;
                else             ypos <= ypos + 1;

assign vsync = ypos < 637 || ypos >= 643;

always @(posedge clk)
        if (xpos < 800 && ypos < 600) begin
                red <= xpos[6] ^ ypos[6];
                green <= 0;
                blue <= ~xpos[5] ^ ypos[5];
        end else begin
                red <= 0;
                green <= 0;
                blue <= 0;
        end

endmodule
```

```
`timescale 10ns / 10ns
module SimpleVGA_tb;
        reg clk = 0;
        always #1 clk = !clk;

        wire hsync;

        SimpleVGA testbench(
                .clk (clk),
                .hsync (hsync)
        );

        initial begin
                $dumpfile("SimpleVGA_tb.vcd");
                $dumpvars(0, testbench);

                #1385280 $finish;
        end

        reg [24:0] counter = 0;
        always @(negedge hsync) begin
                counter = counter + 1;
                $display("HSYNC = %0d @ %0t ns", counter, $time);
        end
endmodule
```

SimpleVGA + **Banc d'essai**

GTKWave



SIMULER POUR DÉBOGUER

ORGANISATION DU BANC D'ESSAI

1) Génération d'une horloge
2) Instanciation de SimpleVGA
3) Lancement de la simulation
4) Création d'un compteur

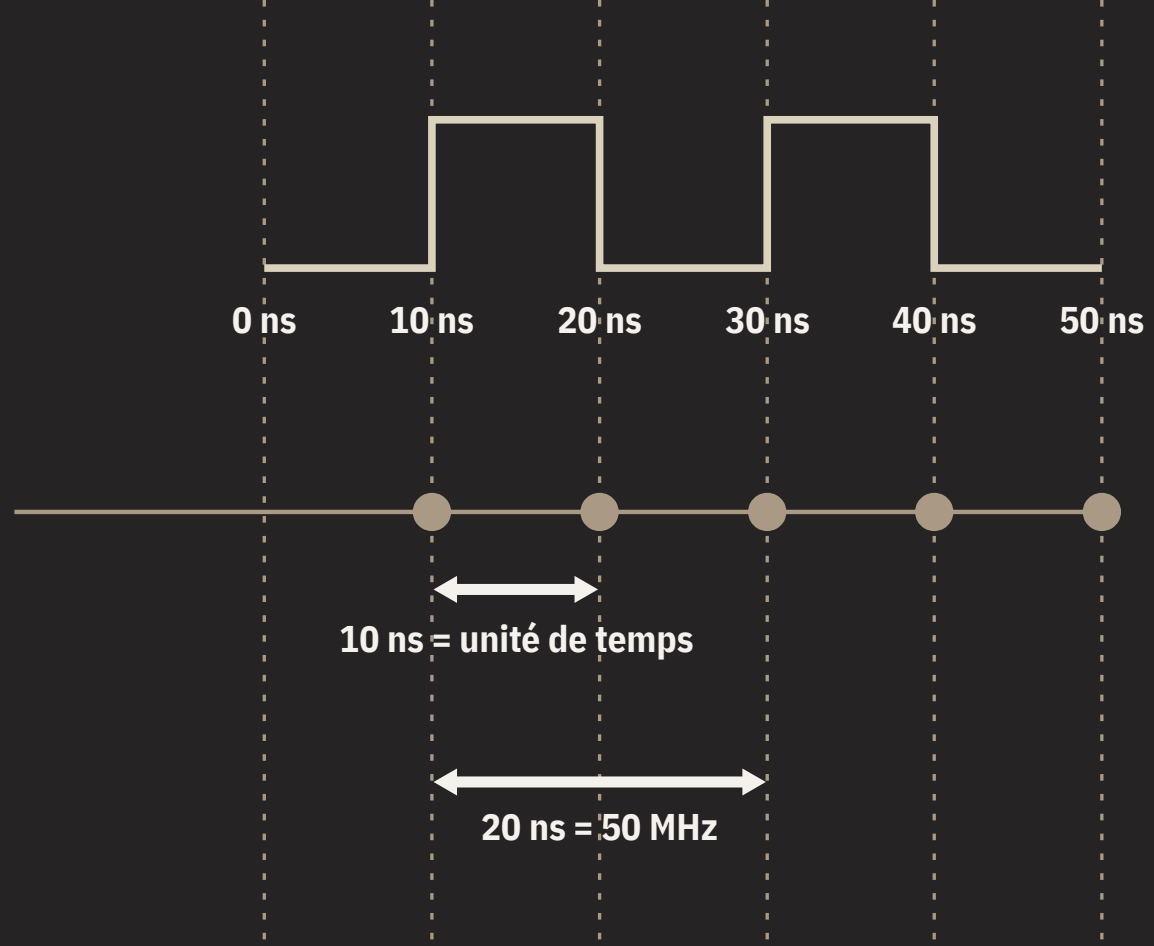
1
```
`timescale 10ns / 10ns
module SimpleVGA_tb;
        reg clk = 0;
        always #1 clk = !clk;

        wire hsync;
```

2
```
        SimpleVGA testbench(
                .clk (clk),
                .hsync (hsync)
        );
```

3
```
        initial begin
                $dumpfile("SimpleVGA_tb.vcd");
                $dumpvars(0, testbench);

                #1385280 $finish;
        end
```

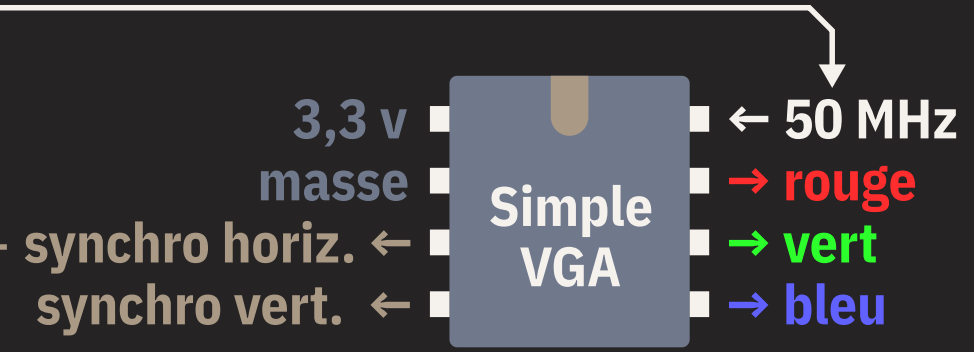
4
```
        reg [24:0] counter = 0;
        always @(negedge hsync) begin
                counter = counter + 1;
                $display("HSYNC = %0d @ %0t ns", counter, $time);
        end
endmodule
```

```
`timescale 10ns / 10ns
module SimpleVGA_tb;
        reg clk = 0;
        always #1 clk = !clk;

        wire hsync;
```



GÉNÉRATION D'UNE HORLOGE

```
SimpleVGA testbench(
        .clk (clk),
        .hsync (hsync)
);
```



INSTANCIATION DE SIMPLEVGA

```
initial begin
        $dumpfile("SimpleVGA_tb.vcd");
        $dumpvars(0, testbench);

        #1385280 $finish;
end
```

bloc exécuté une seule fois

tâche système

sauve tous les signaux de testbench

termine la simulation après
20 ns × 1040 × 666 = 13 852 800 ns

$$\simeq \frac{1}{72}\ \text{s}$$

LANCEMENT DE LA SIMULATION

```
reg [24:0] counter = 0;
always @(negedge hsync) begin
        counter = counter + 1;
        $display("HSYNC = %0d @ %0t ns", counter, $time);
end
```

CRÉATION D'UN COMPTEUR

Ligne de commande

```
$ iverilog -o SimpleVGA_tb SimpleVGA_tb.v SimpleVGA.v
```

COMPILATION DU BANC D'ESSAI

Ligne de commande

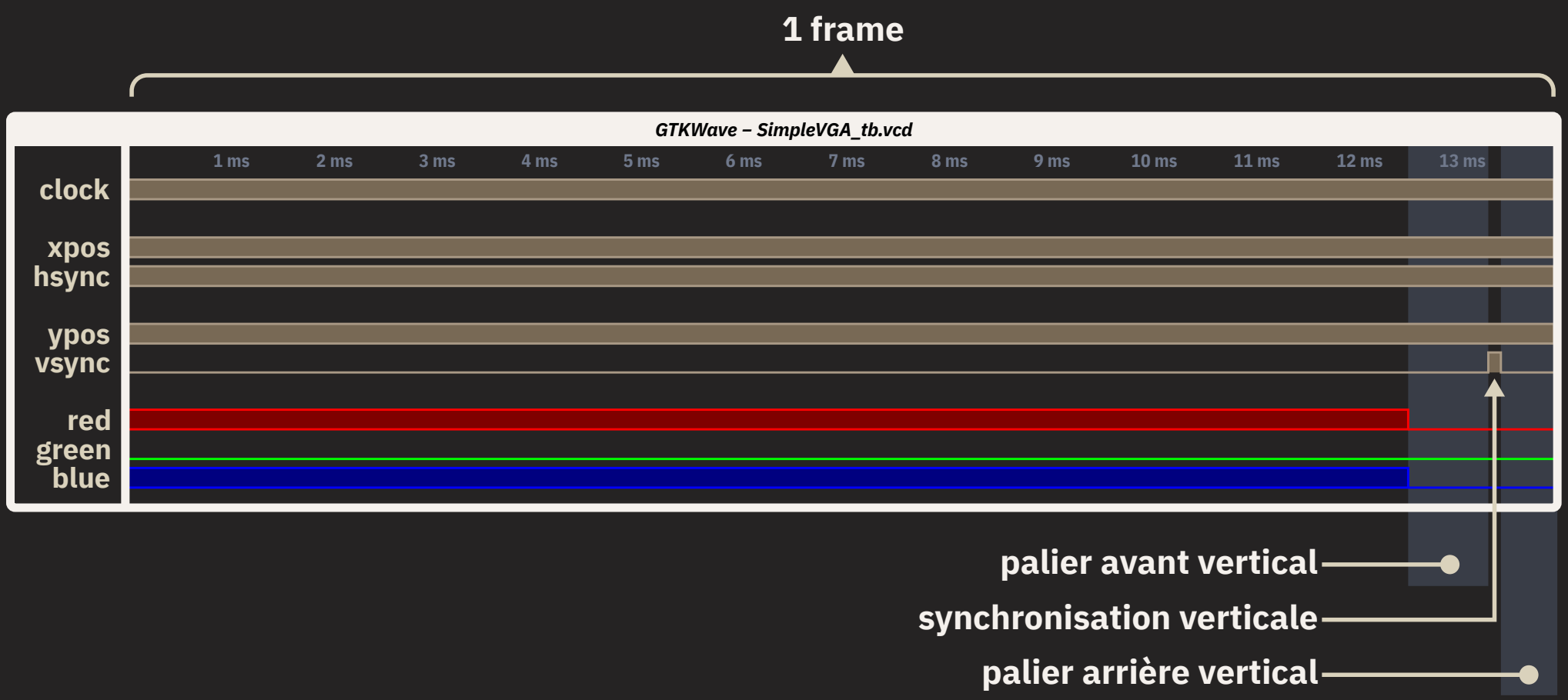
```
$ iverilog -o SimpleVGA_tb SimpleVGA_tb.v SimpleVGA.v
$ ./SimpleVGA_tb
VCD info: dumpfile SimpleVGA_tb.vcd opened for output.
HSYNC = 1 @ 1711 ns
HSYNC = 2 @ 3791 ns
HSYNC = 3 @ 5871 ns
# ...
HSYNC = 664 @ 1380751 ns
HSYNC = 665 @ 1382831 ns
HSYNC = 666 @ 1384911 ns
```

EXÉCUTION DE LA SIMULATION

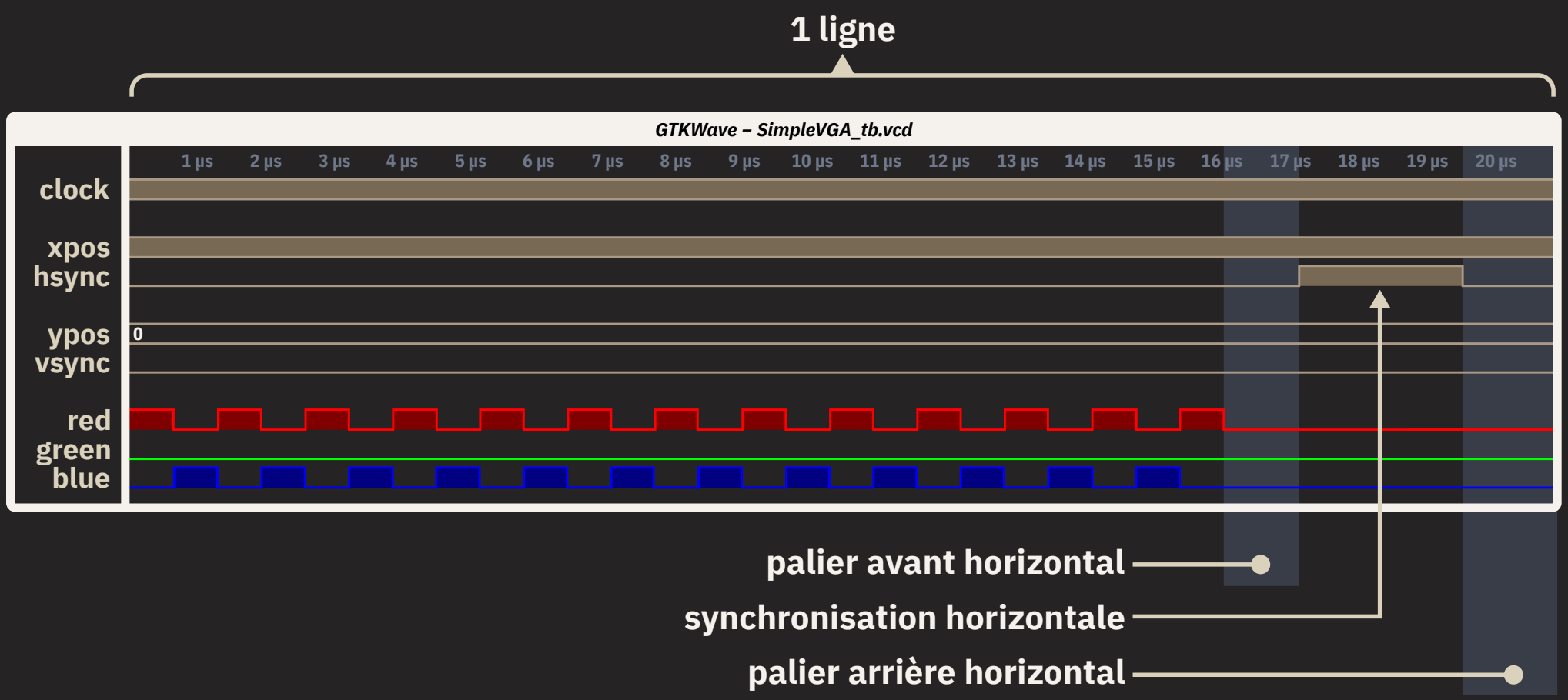
Ligne de commande

```
$ iverilog -o SimpleVGA_tb SimpleVGA_tb.v SimpleVGA.v
$ ./SimpleVGA_tb
VCD info: dumpfile SimpleVGA_tb.vcd opened for output.
HSYNC = 1 @ 1711 ns
HSYNC = 2 @ 3791 ns
HSYNC = 3 @ 5871 ns
# ...
HSYNC = 664 @ 1380751 ns
HSYNC = 665 @ 1382831 ns
HSYNC = 666 @ 1384911 ns
$ gtkwave SimpleVGA_tb.vcd
```

LANCEMENT DE GTKWAVE

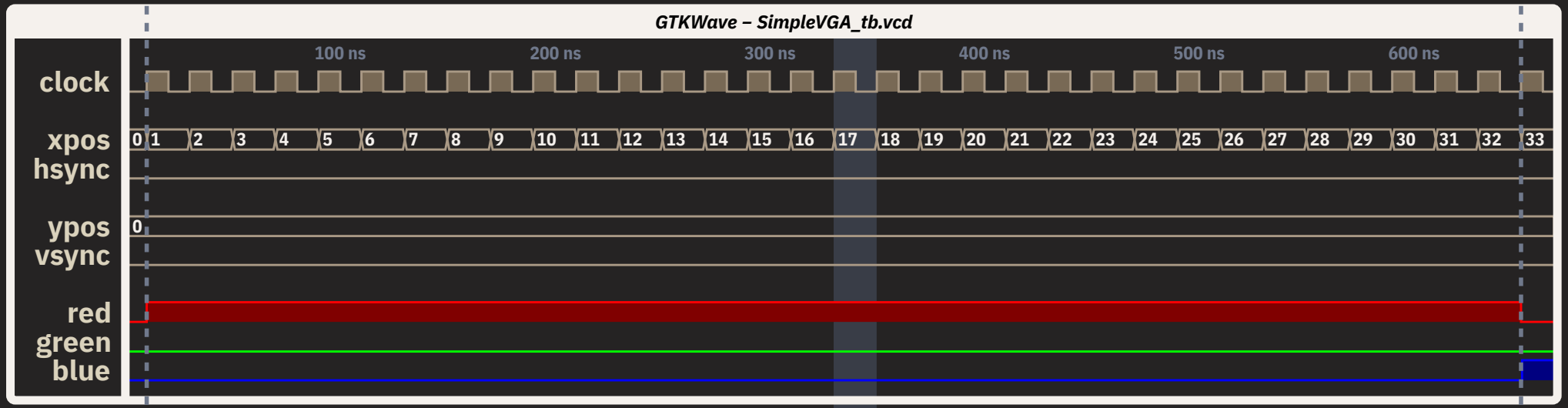


ÉVOLUTION DES SIGNAUX (FRAME)



ÉVOLUTION DES SIGNAUX (LIGNE)

32 cycles

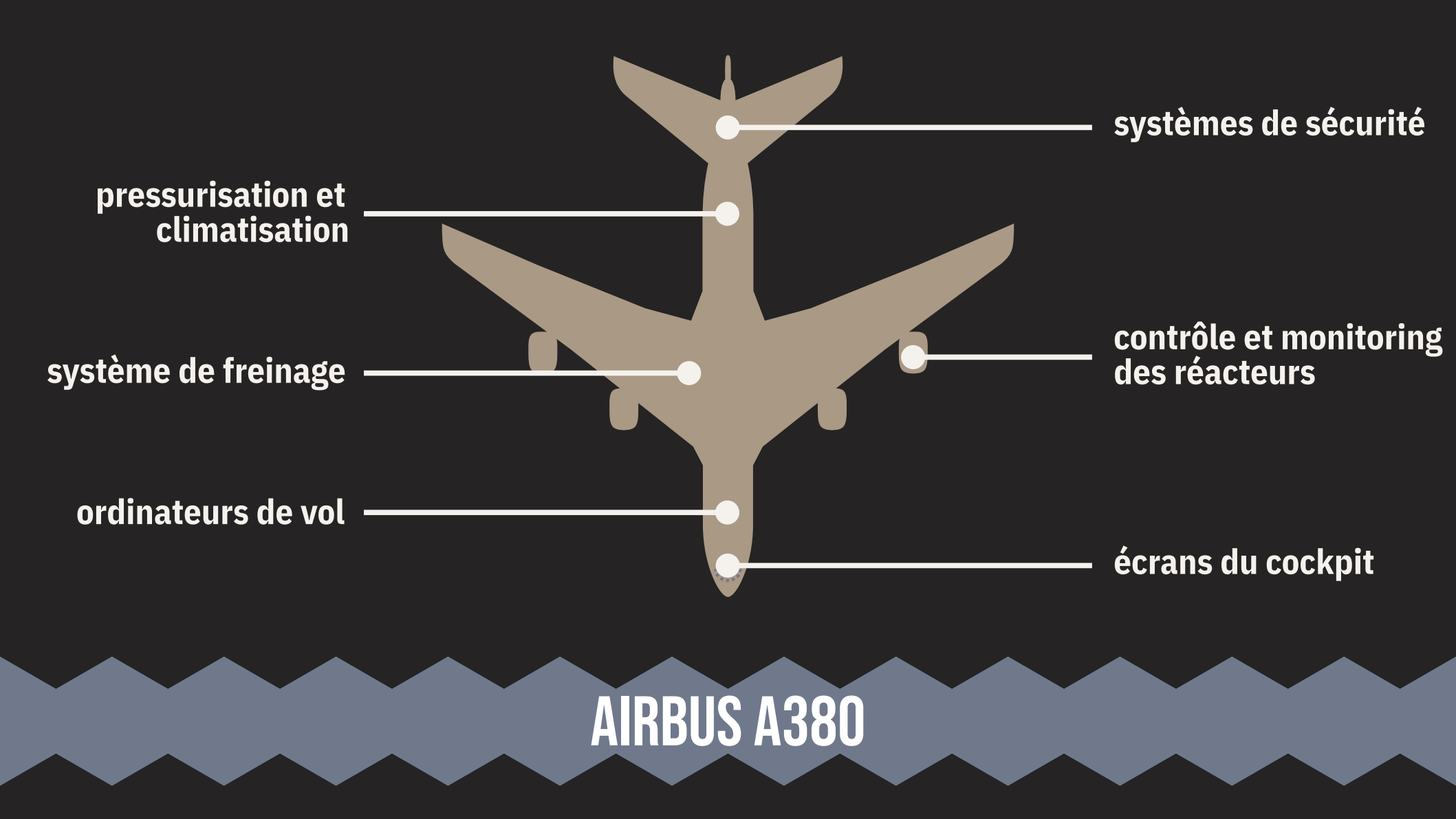


1 cycle = 20 ns / 50 MHz = 1 pixel

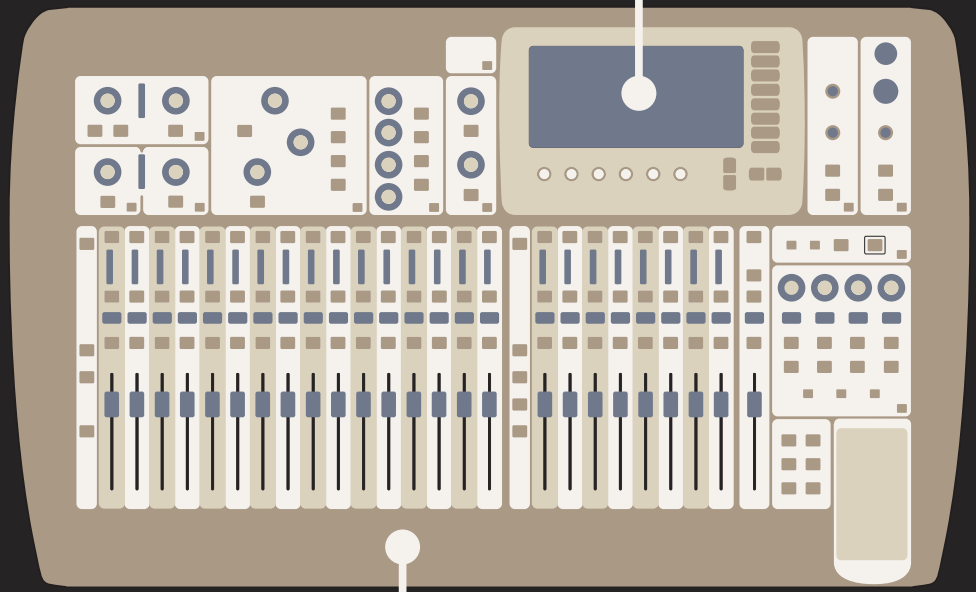
ÉVOLUTION DES SIGNAUX (HORLOGE)

ET MAINTENANT ?

QUELQUES EXEMPLES D'UTILISATION


systèmes de sécurité
pressurisation et climatisation
contrôle et monitoring des réacteurs
système de freinage
ordinateurs de vol
écrans du cockpit
AIRBUS A380

effets en temps réel

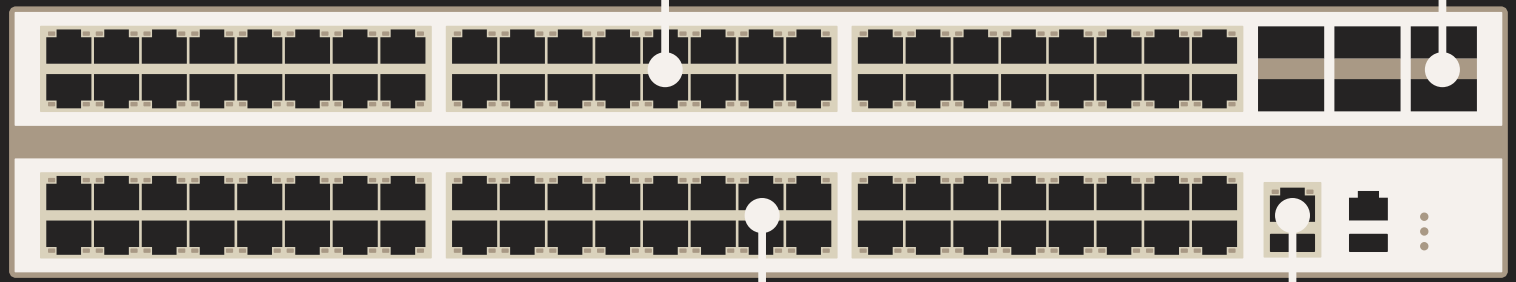


mixage de nombreuses entrées

TABLE DE MIXAGE BEHRINGER X32

très faible latence

très haut débit



gestion de nombreuses entrées

mises à jour

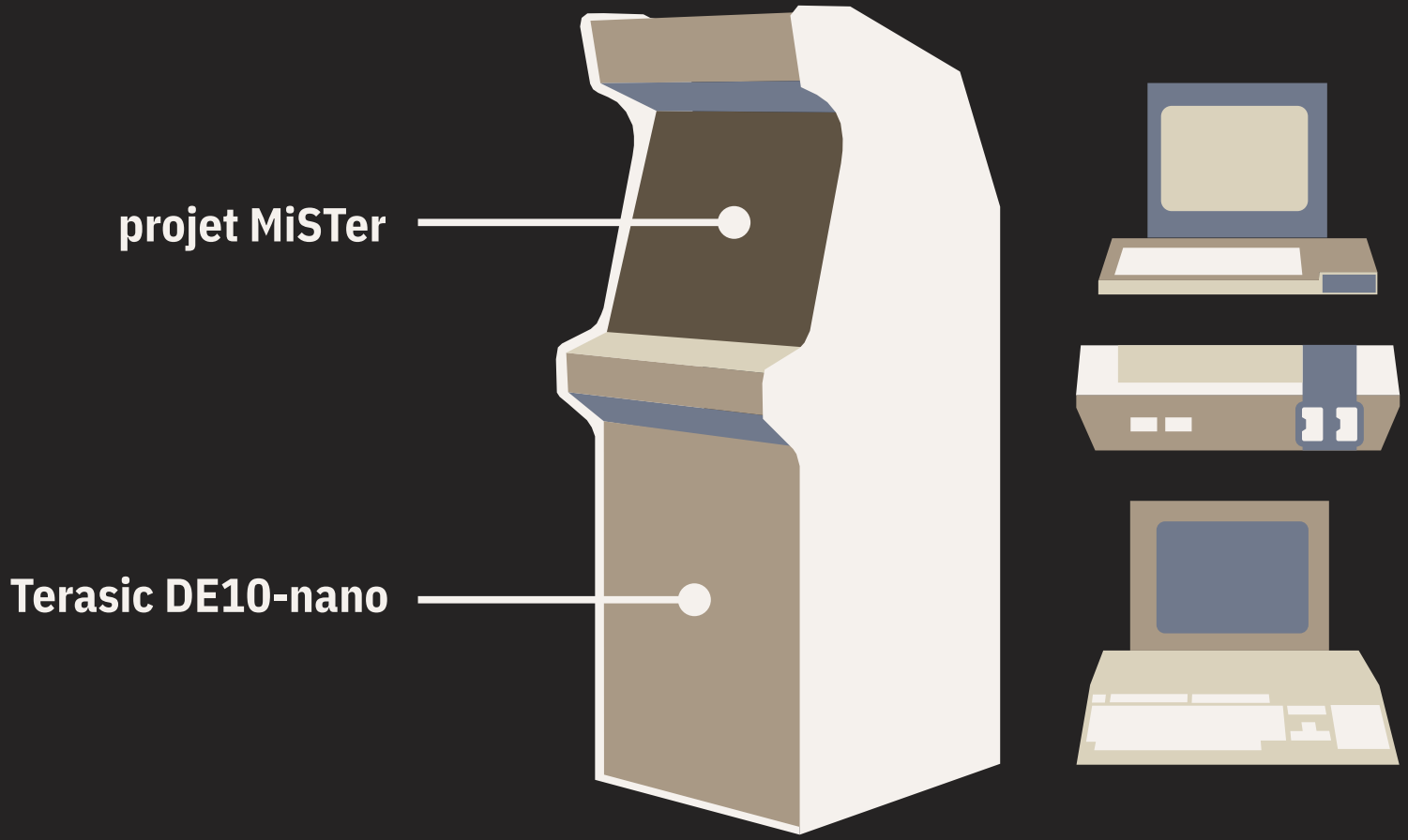
SWITCH CISCO

traitement d’image
après acquisition

traitement des
données brutes

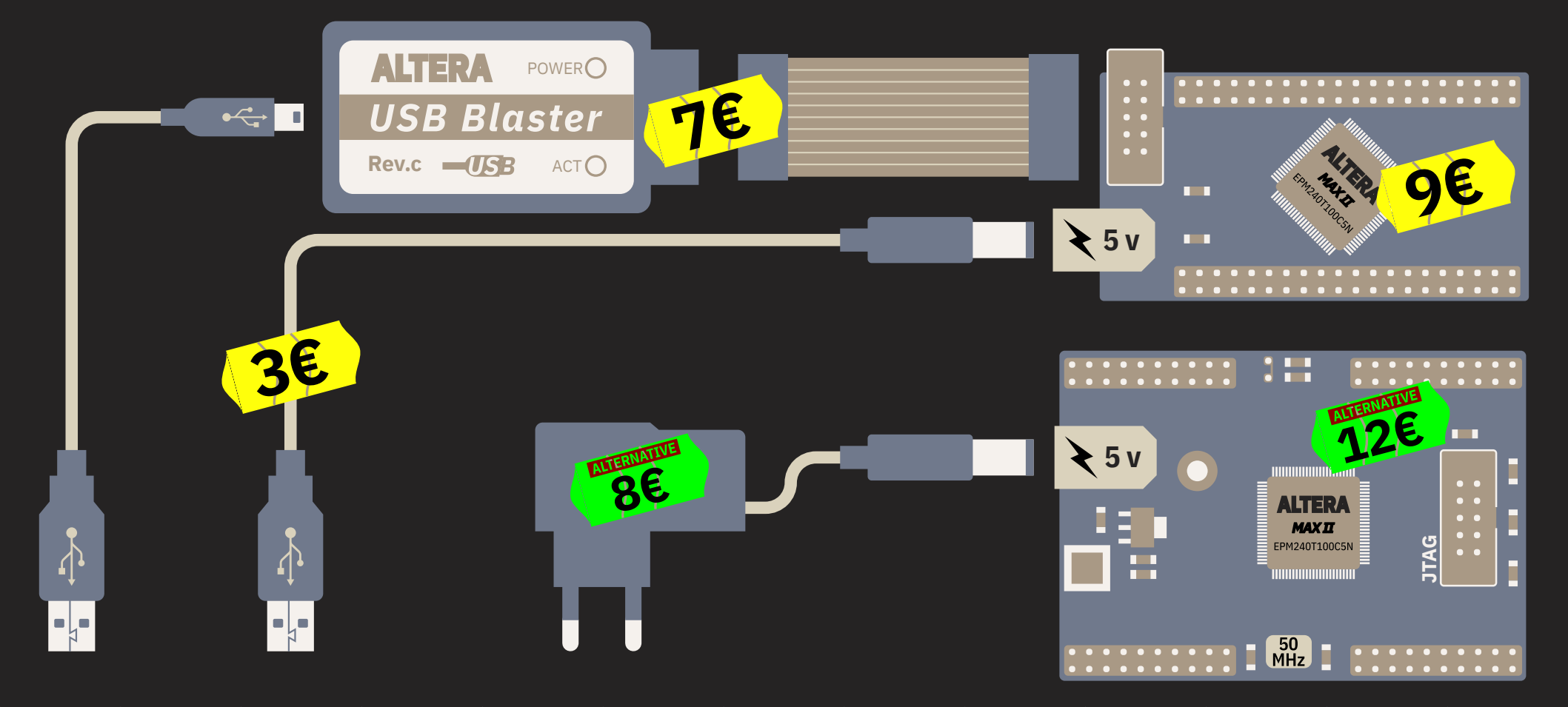
IMAGERIE MÉDICALE : IRM


SYN flood
UDP flood
TCP flood
VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC - VAC -
OVHcloud
Intel Stratix V
Xilinx Virtex UltraScale+
SYSTÈME ANTI-DDOS D'OVHCLOUD



ÉMULATION FINE D'ANCIENNES PLATEFORMES

PAR OÙ COMMENCER ?



AVEC UN BUDGET DE 20€

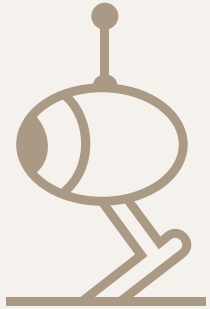
AVANTAGES/INCONVÉNIENTS DES FPGA

Inconvénients des FPGA

- Autre façon de programmer
  - paradigme
  - temps de compilation
  - débogage
- Positionnement
  - ASIC
  - GPU
  - microcontrôleur
- Ticket d'entrée
  - coût des logiciels
  - coût des circuits
- Écosystème limité
  - open source peu présent
  - disponibilité des compétences
  - OpenCL

AVANTAGES DES FPGA

- Plus proche de l’électron
  - flexibilité des entrées/sorties
  - moins de composants
  - consommation électrique
- Puissance de calcul
- Précision du signal
  - comportement déterministe
  - faible latence
- Reconfigurable
- Sécurité
  - pas de dépassement
  - offuscation ?



Merci de votre attention !

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